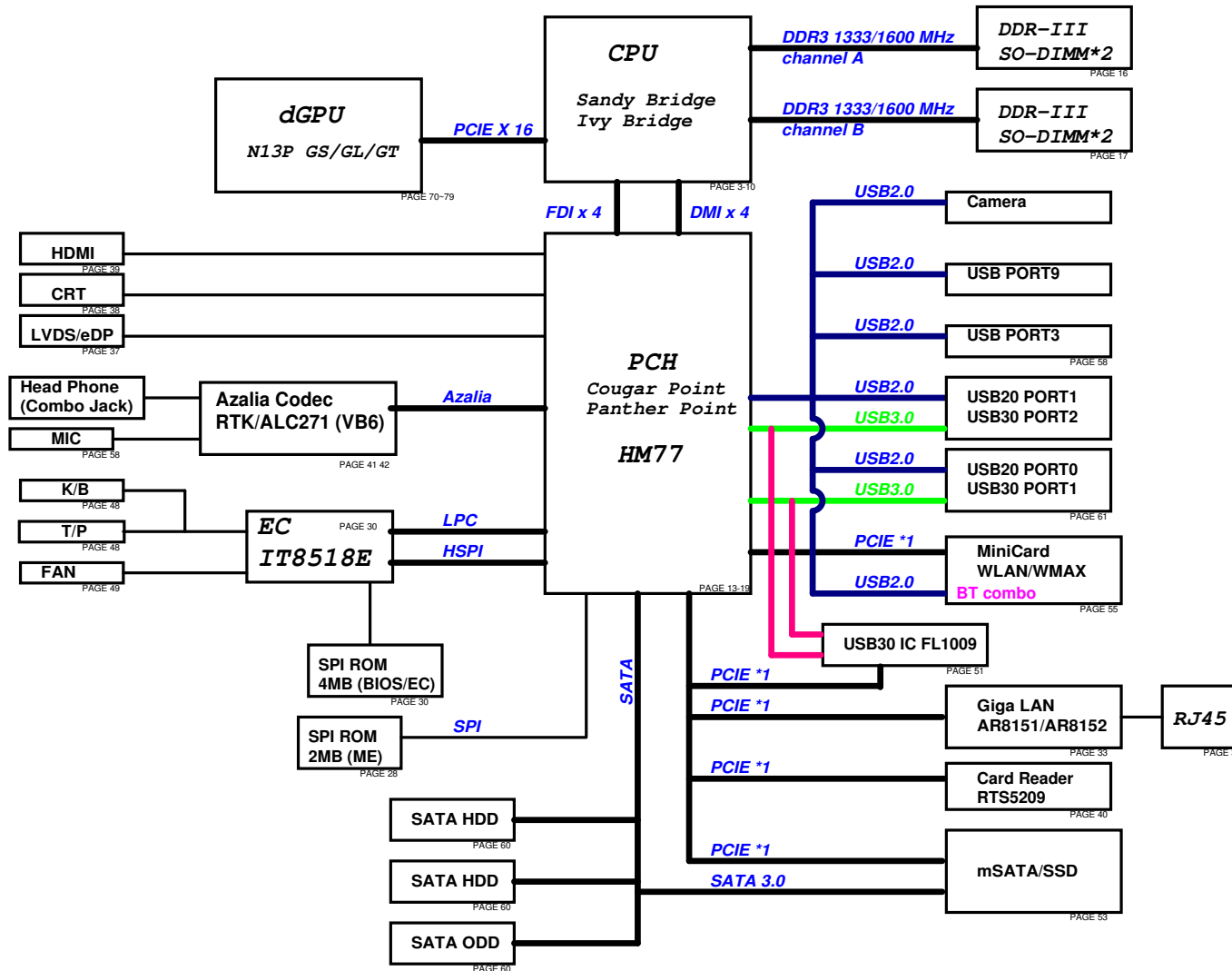


VA70 BLOCK DIAGRAM



POWER

CPU VCORE	PAGE 80
SYSTEM, +3V, +5V	PAGE 81
+VCCP & +VCCP_VT	PAGE 82
DDR & VTT	PAGE 83
2.5V & 1.5VS & 1.1VS	PAGE 84
SMART CHARGER	PAGE 88
POWER DETECT	PAGE 90
LOAD SWITCH	PAGE 91
POWER PROTECT	PAGE 92

VGA POWER

GPU VCORE	PAGE 80
+1.05VS_VGA	
+1.5VS_VGA	
+3VS_VGA	
+12VS_VGA	
LOAD SWITCH	PAGE 91
POWER PROTECT	PAGE 92

Power Rails

Sleep State	RTC	VA	VSUS	V	VS
S0	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
S4	ON	ON	ON	OFF	OFF
S5/ AC	ON	ON	ON	OFF	OFF
S5/ DC	ON	ON	OFF	OFF	OFF

PCIe Port

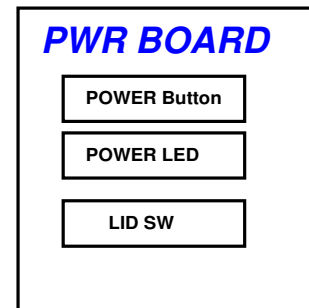
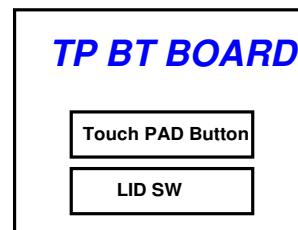
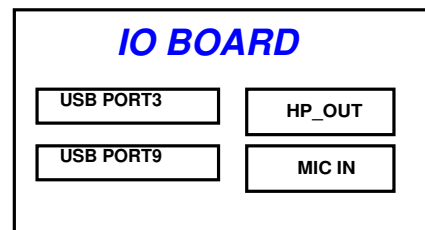
PCIe_P1	CARDREADER
PCIe_P2	Mini CARD (WLAN)
PCIe_P3	mSATA
PCIe_P4	USB30
PCIe_P5	
PCIe_P6	LAN

USB20 PORT

USB P00	External MB
USB P01	External MB
USB P02	
USB P03	External DB
USB P04	
USB P05	BT
USB P08	Camera
USB P09	External DB
USB P10	
USB P11	SSD
USB P12	
USB P13	

SATA PORT

SATA P0	HDD 1
SATA P1	HDD 2
SATA P2	ODD 3
SATA P3	mSATA
SATA P4	
SATA P5	



PEGATRON

Title : BLOCK DIAGRAM

BU1-RD Div.1-HW RD Dept.1

Engineer: Wing_Cheng

Size Custom

Project Name

BA52HR/CR

Rev

Date: Friday, February 03, 2012

Sheet

1

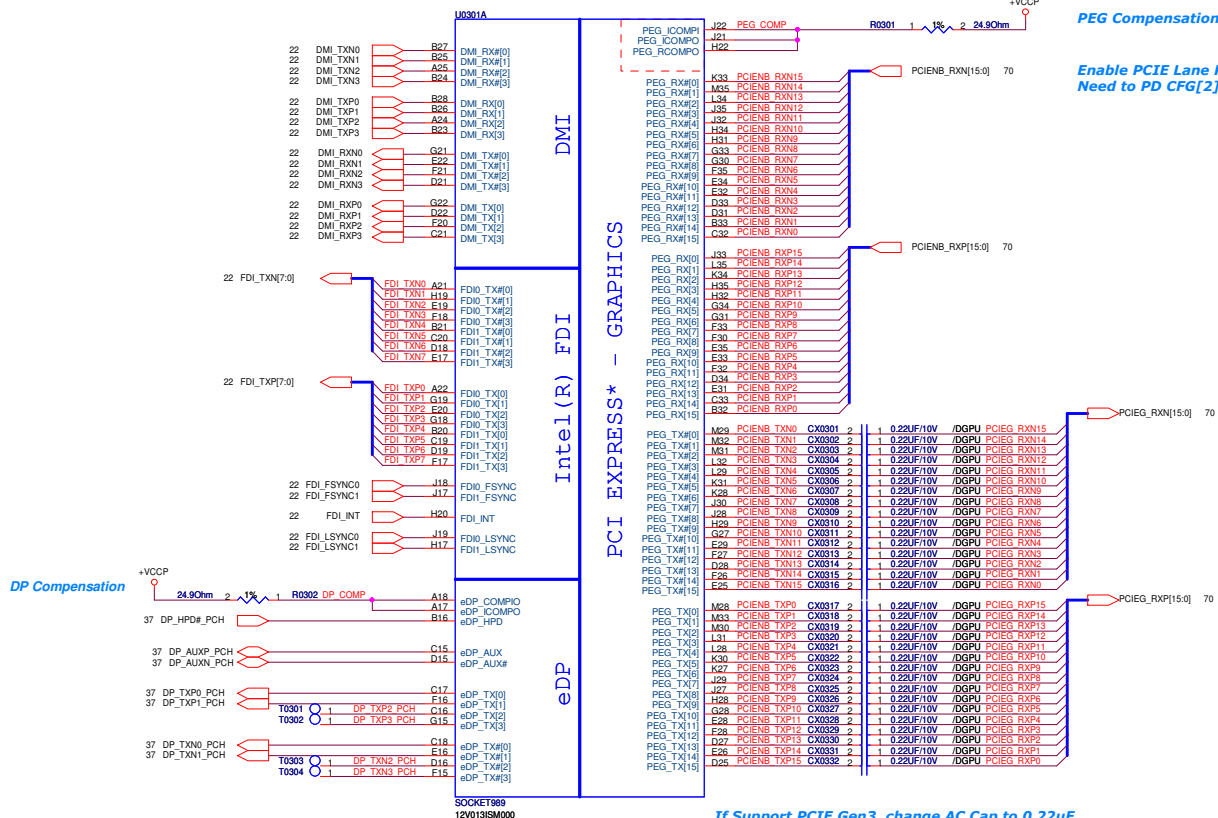
of

77

BOM optional	Remark
N/A	For 上件
/ABCT	For ABCT，上件
/niAMT	For no iAMT，上件
/HOME	For 上件
/HR	For Huron River，上件
/Non_HSPI	For ROM SETTING，上件
Entry	For 上件
Main	For 上件
/USB20	For USB 2.0，上件
/HSPI	For 不上件
/HDMI	For HDMI用，不上件
/TP1_AUD	For power control，不上件
/TP1_BT	For power control，不上件
/TP1_CAMERA	For power control，不上件
/TP1_CR	For power control，不上件
/TP1_LAN	For power control，不上件
/TP1_ODD	For power control，不上件
/TP1_WLAN	For power control，不上件
/THERM	For Palm Rest溫度，不上件
/usb30	For USB 3.0，不上件
/ZPODD	For ODD battery saving使用Mount R5108，不上件
@	For 不上件
@/MP	For debug port, MP不上件
/BT270	視keypat list而定
/COMBO_BT	視keypat list而定
/SATA+	For Sata Repeater, SR先上件

PEGATRON		Title : System Setting	
PEGATRON COMPUTER INC		Engineer: Wing_Cheng	
Size A	Project Name BA52HR/CR		Rev 1.0
Date: Friday, February 03, 2012		Sheet 2	of 94

+VCCP 4.6,7,25,26,27,37,47,53,82



1201-006D000 - 988B for Huron River

If Support PCIe Gen3, change AC Cap to 0.22uF

PEG Compensation

Enable PCIe Lane Reversal
Need to PD CFG[2]

25 H_SNB_IVB#

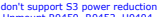


Power good for +1.5V_VCCDDQ (delay > 100ns)



Frank \

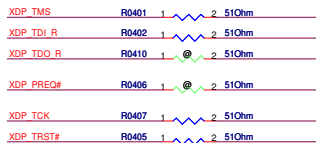
0506 EVERST check

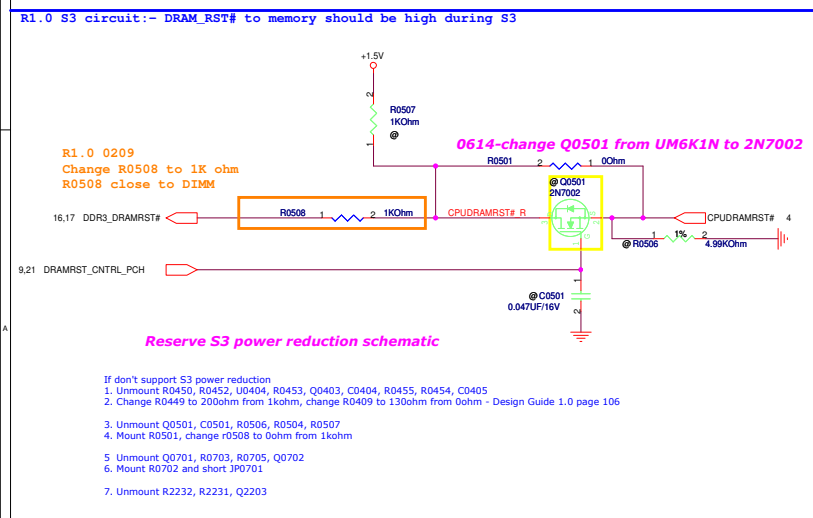
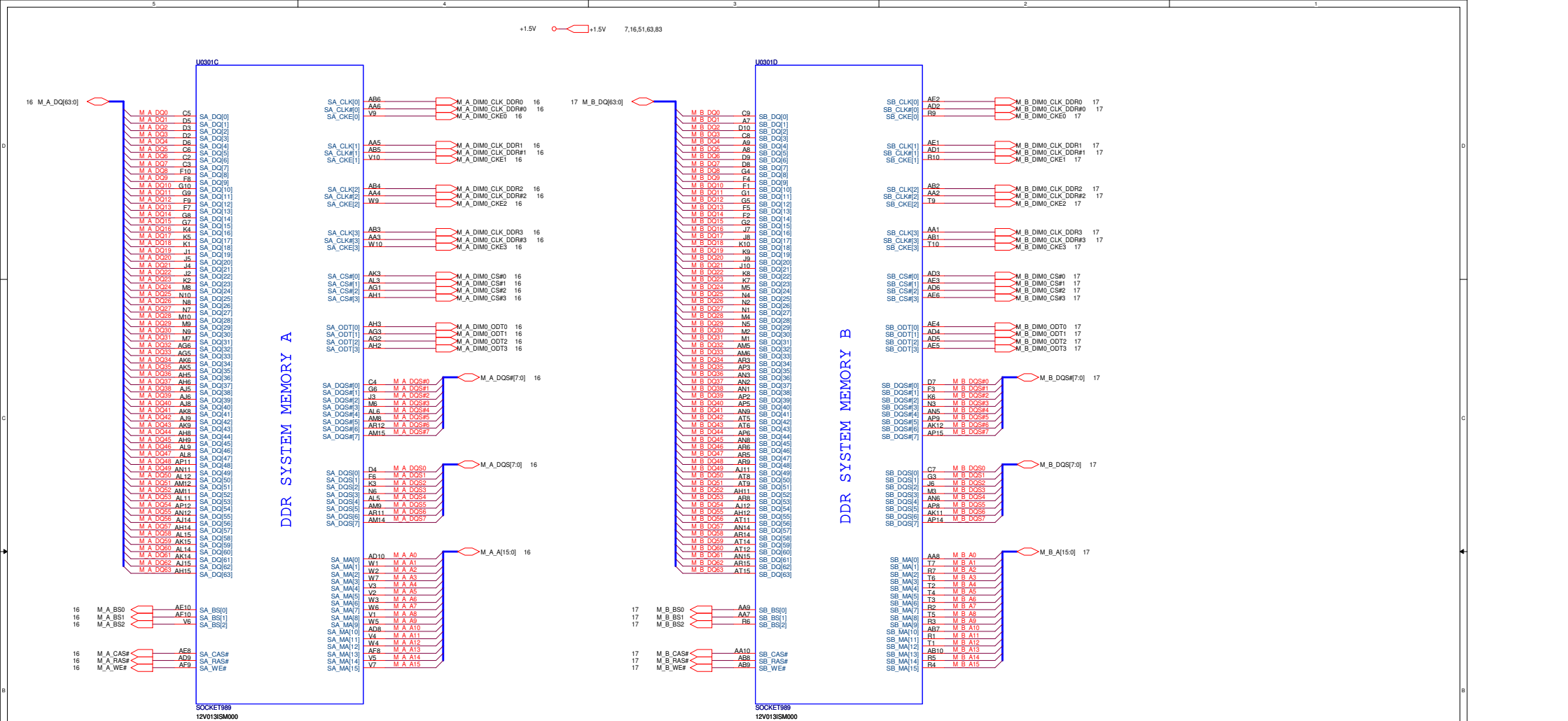


Unmount Q0501, C0501, R0506, R0504, R0507



R1.0 PU/PD for JTAG signals





Vcc for processor core
Voltage range: 0.3 ~ 1.52V

POWER

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

Voltage for the memory controller and
shared cache defined at the
motherboard VCCIO_SENSE and
VSS_SENSE_VCCIO

ICCMAX_VCCIO 8.5A

R1.0 0126
Intel Comments

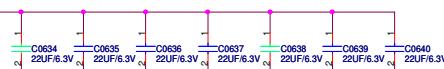
R1.0 0126
Intel Comments

Frank
20110602 check pull up/pull down reserve power schematic or not.

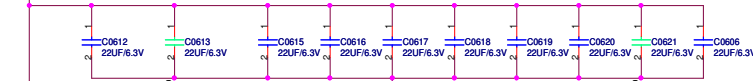
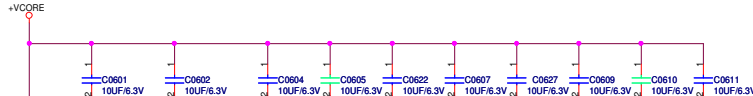
Frank
20110516 Change VCCP_SENSE to VCCIO_SENSE
and change VSSP_SENSE to VSSIO_SENSE
for meet power schematic.

Frank
20110516 Remove R0601 and R0604, because Power is already reserved

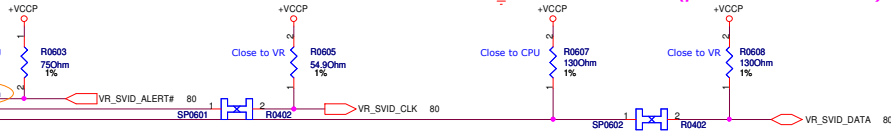
0614-Remove C0641 and nostuff C0651,C0647,C0658



0622-Remove CE0603(powre schematic reserve)



0622-Remove CE0601(powre schematic reserve)



R1.0 0126
Intel Comments

+VCCP 3.4,7,25,26,27,37,47,63,82
+VCCORE 63,80

Check net name??

HR_Decoupling guide from Intel (POWER + EE)
+VCCP 22uF * 19pcs (7 nostuff)
330uF * 3pcs

EIH31/30 (EE)
+VCCP 10uF * 19pcs (2pcs no stuff)
22uF * 10 pcs (total no stuff)
330 uF * 1pcs Power support

CR_Decoupling guide from Intel (POWER + EE)
+VCCP 22uF * 19pcs (7 nostuff)
330uF * 3pcs

Decoupling guide for Everest (EE)
+VCCP 22uF * 19pcs (7 no stuff)
330uF * 1pcs (1 no stuff)=>JE31HR/CR
power support

HR_Decoupling guide from Intel (POWER + EE)
+VCC_CORE 22uF * 16pcs
10uF * 10pcs
470uF * 4pcs

EIH31/30
+VCC_CORE 22uF * 14pcs(6pcs unmount)
10uF * 16pcs (4pcs unmount)
470uF * 2pcs (Power support)

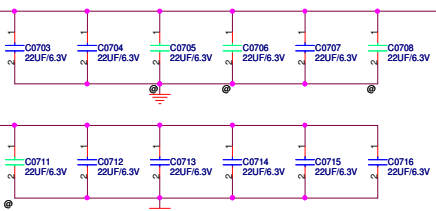
CR_Decoupling guide from Intel (POWER + EE)
+VCC_CORE 22uF * 16pcs
10uF * 10pcs
470uF * 4pcs

Decoupling guide for Everest (EE)
+VCC_CORE 22uF * 16pcs (8 nostuff)
10uF * 10pcs (3 nostuff)
470uF * 1pcs=>JE31HR/CR power support

SV-QC ICMAX_VA_XG 33A
SV-DC ICMAX_VA_XG 33A

+VGFX_CORE

Graphics core voltage
Voltage range: 0 - 1.52V



0622-Remove CE0705(powre schematic reserve)

HR_Decoupling guide from Intel (POWER + EE)

+VGFX_CORE 22uF * 12pcs
470uF * 2pcs

EIH31/30

+VCCP 22uF * 16 pcs (6 unmount)
330uF * 1pcs (power support)
470uF * 1pcs (EIH31 Del 470uF For Layout)

CR_Decoupling guide from Intel (POWER + EE)

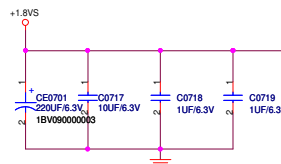
+VGFX_CORE 22uF * 12pcs
470uF * 2pcs

Decoupling guide for Everest (EE)

+VGFX_CORE 22uF * 12pcs (2 nostuff)
470uF * 1pcs (JE31HR/CR power support)

PLL supply voltage (DC + AC
specification)

ICMAX_VCCPLL 1.2A



HR_Decoupling guide from Intel (POWER + EE)

+1.8VS 1uF * 2pcs
10uF * 1pcs
330uF * 1pcs

EIH31/30

+1.8VS 1uF * 2pcs
10uF * 1pcs
2.2uF*1pcs
4.7uF*1pcs
22uF * 1pcs (un-mount)

CR_Decoupling guide from Intel (POWER + EE)

+1.8VS 1uF * 2pcs
10uF * 1pcs
330uF * 1pcs

Decoupling guide from Everest (EE)

+1.8VS 1uF * 2pcs
10uF * 1pcs
100uF * 1pcs

POWER

U0301G

VAXG1
VAXG2
VAXG3
VAXG4
VAXG5
VAXG6
VAXG7
VAXG8
VAXG9
VAXG10
VAXG11
VAXG12
VAXG13
VAXG14
VAXG15
VAXG16
VAXG17
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VAXG35
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VAXG38
VAXG39
VAXG40
VAXG41
VAXG42
VAXG43
VAXG44
VAXG45
VAXG46
VAXG47
VAXG48
VAXG49
VAXG50
VAXG51
VAXG52
VAXG53
VAXG54

VCCPL1
VCCPL2
VCCPL3
VCCSA1
VCCSA2
VCCSA3
VCCSA4
VCCSA5
VCCSA6
VCCSA7
VCCSA8
VCCSA_SENSE
FC_C22
VCCSA_VDI1

SOCKET988
12V013ISM000

SENSE
LINES

VREF

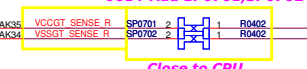
DDR3 -1.5V RAILS

SA RAIL

MISC

R1.0 Add net name, Joyoung 0621

0614-Add SP0701,SP0702

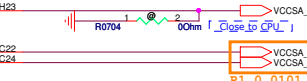
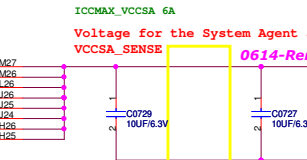
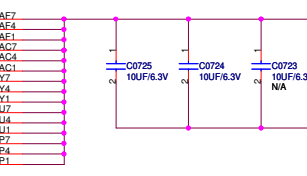


Close to CPU

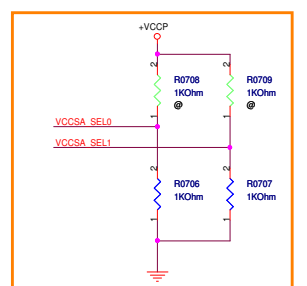


DDR3 Reference Voltage

Reserve S3 power reduction schematic



R1.0 0209
Intel Comments



+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

HR_Decoupling guide from Intel (POWER + EE)
+VCCSA 10uF * 3pcs
330uF * 1pcs

EIH31/30

+VCCSA 10uF * 4pcs (2 nostuff)
100uF * 1pcs

CR_Decoupling guide from Intel (POWER + EE)

+VCCSA 10uF * 3pcs
330uF * 1pcs

Decoupling guide for Everest (EE)

+VCCSA 10uF * 3pcs (1 nostuff)
100uF * 1pcs

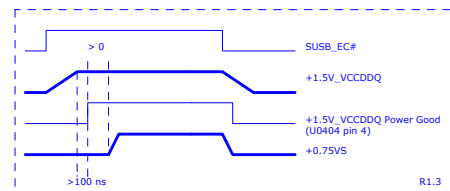
+VCCP 3,4,6,25,26,27,37,47,63,82
+1.5V 5,16,51,63,83
+VCCSA 85
+1.8VS 25,26,63,84
+VGFX_CORE 63,80
+1.5V_VCCDDQ 4
+V_SM_VREF 18

PS_S3CNTRL_1.5V 22

ICMAX_VDDQ 5A Joyoung 0613
Reduce to 5A (EDS R2.1)

Processor I/O supply
voltage for DDR3
(DC + AC specification)

0614-Change JP(3MM_OPEN_5MIL)



HR_Decoupling guide from Intel (POWER + EE)

+VDDQ 10uF * 6pcs
330uF * 1pcs

EIH31

+VDDQ 10uF * 6pcs (3 nostuff)
220uF * 1pcs

CR_Decoupling guide from Intel (POWER + EE)

+VDDQ 10uF * 6pcs
330uF * 1pcs

Decoupling guide for Everest (EE)

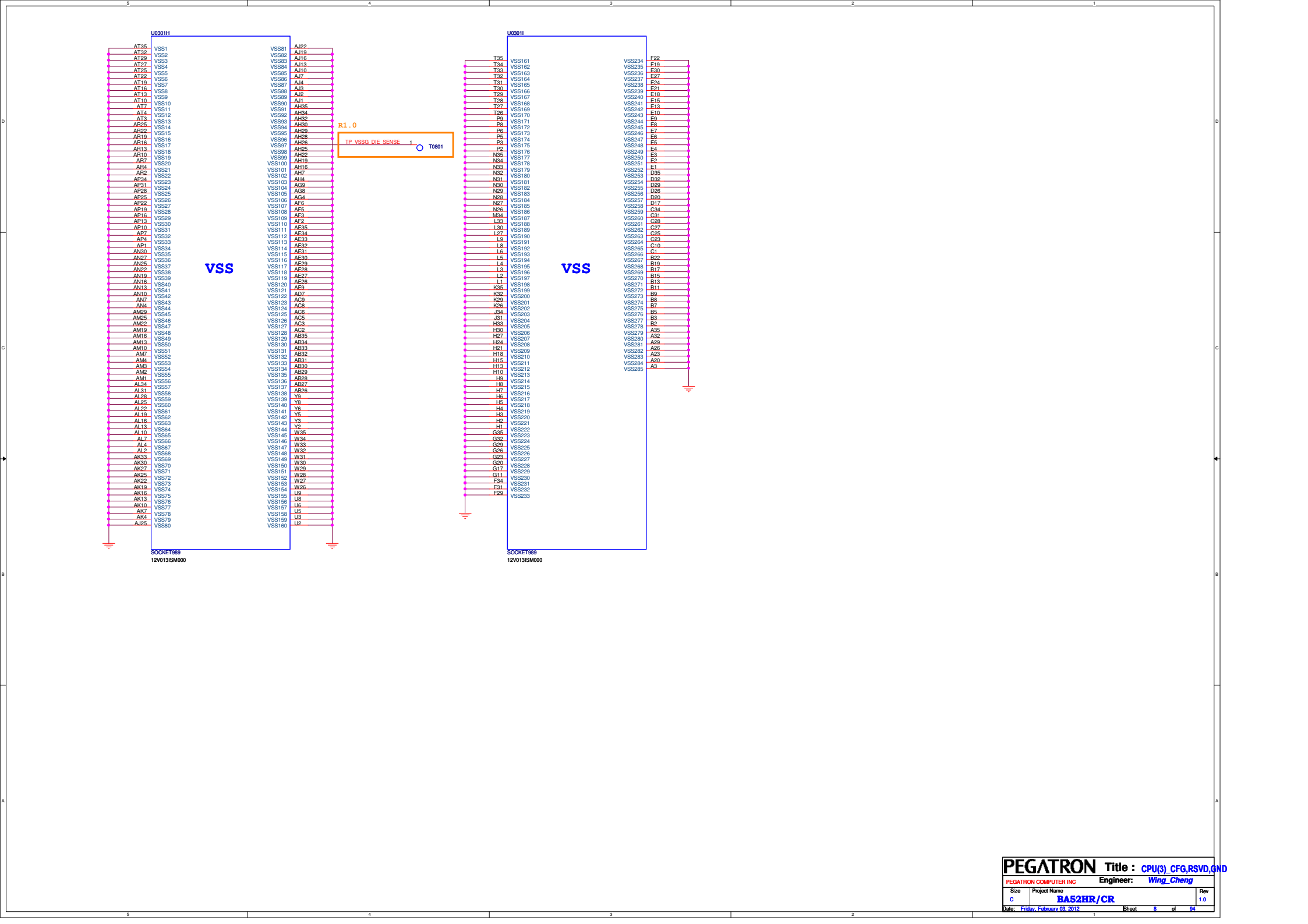
+VDDQ 10uF * 6pcs (3 nostuff)
220uF * 1pcs

PEGATRON Title : CPU(4)_PWR

PEGATRON COMPUTER INC Engineer: Wing Cheng

Size C Project Name BA52HR/CR Rev 1.0

Date: Friday, February 03, 2012 Sheet 7 of 94



CFG strapping information:

CFG[2]: PCIE Static Numbering Lane Reversal- CFG[2] is for the 16x

- 1: (Default) Normal Operation, Lane # definition matches socket pin map definition
- 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG[4]: Embedded DisplayPort Detection

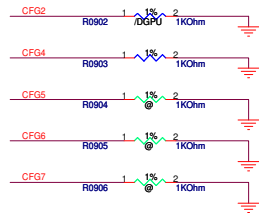
- 1: (Default) Disabled ; No Physical Display Port attached to Embedded DisplayPort
- 0: Enabled ; An external Display Port device is connected to the Embedded Display Port

CFG[6:5]: PCI Express Port Bifurcation Straps

- 11 : (Default) x 1 6
- 10 : x 8 , x 8
- 01 : Reserved
- 00 : x 8 , x 4 , x 4

CFG[7]: PEG DEFER TRAINING

- 1: (Default) PEG Train immediately following xxRESETB de assertion
- 0: PEG Wait for BIOS training

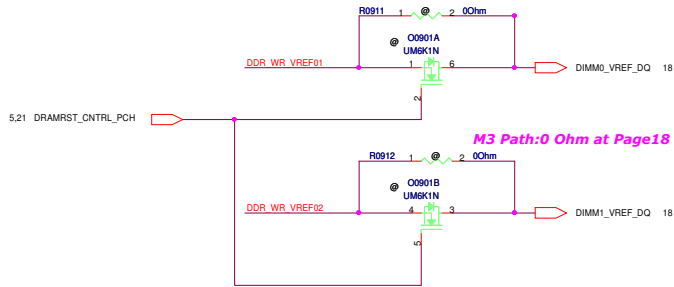


Power schematic reserve 1.0V or not??

+VCCIO_SEL	
1	1.05V
0	1.00V

IVB VCCIO for Mobile and Desktop is changed from 1.0v to 1.05v, same as PPT VCCIO. (461017 WW23'11)

PROCESSOR DRIVEN Vref PATH WAS STUFFED BY DEFAULT:



Reserve S3 power reduction schematic

M3: Processor Generated SO-DIMM VREFDQ
- New Requirement

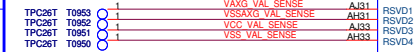
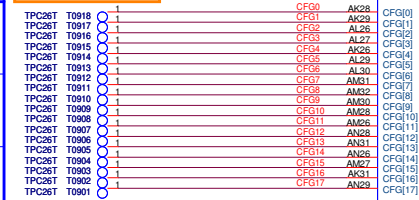
Sandy Bridge CPU Only: M1 Implementation
Sandy Bridge/Ivy Bridge CPU: M1 and M3 Implementation

R1.0

Add CFG0

Frank

0516 Remove CFG0 to XDP



R1.0 0126

DIMM0_VREF_DQ_R Pull Down 1k ohm
DIMM1_VREF_DQ_R Pull Down 1k ohm
Design Guide 1.0 P.89 Figure 44 (436735)

R1.0 0111

Delete VCCIO_SEL_Joyoung0614
TPC26T T0955

Frank
20110516 Change VCCP_SEL to VCCIO_SEL for
meeting Power schematic defined

U0301E

Frank

0516 Remove CFG0 to XDP

0516 Remove CFG0 to XDP

0516 Remove CFG0 to XDP

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0516 Remove CFG0 to XDP

0516 Remove CFG0 to XDP

RESERVED

KEY

SOCKET989

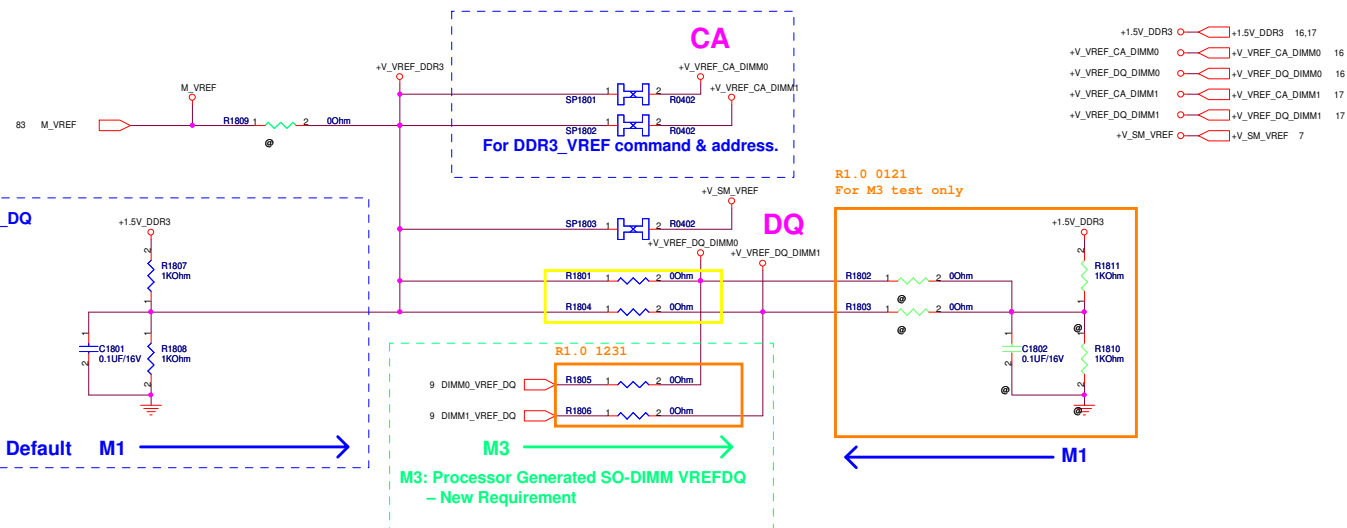
12V013ISM000

+VTT_PCH_ORG +VTT_PCH_ORG 22,26,27
+3VSUS +3VSUS 4,22,24,27,28,30,33,65,81,85,92
+VCCP +VCCP 3,4,6,7,25,26,27,37,47,63,82
+3VS +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,37,38,39,40,41,47,48,49,53,55,60,63,66,69,91,92

CPU XDP connector

PCH XDP connector

DDR3 Vref



If support M1 :(Sandy Bridge CPU Only)

1. Un mount R1802,R1803,R1805,R1806,R1810,R1811,C1802
2. Mount R1801,R1804

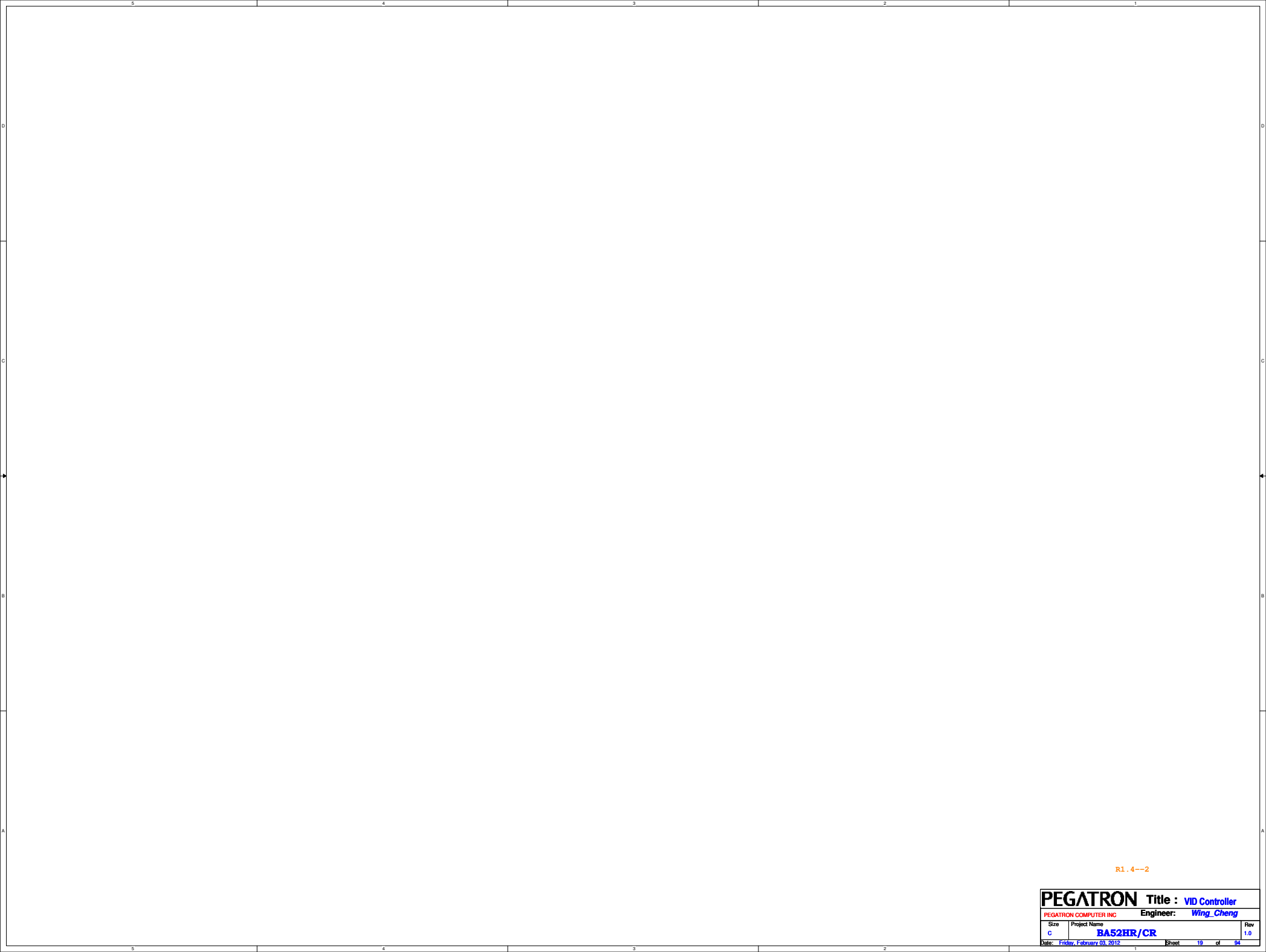
==>CA and DQ are the same path

If support M1 and M3 :(Sandy Bridge/Ivy Bridge CPU)

1. Mount R1802,R1803,R1805,R1806,R1810,R1811,C1802
2. Un mount R1801,R1804

==> CA and DQ are separate path

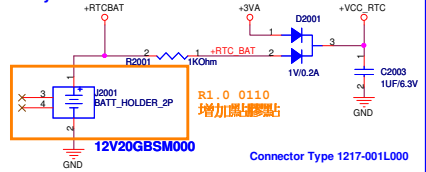
Sandy Bridge CPU Only: M1 Implementation
Sandy Bridge/Ivy Bridge CPU: M1 and M3 Implementation



R1.4--2

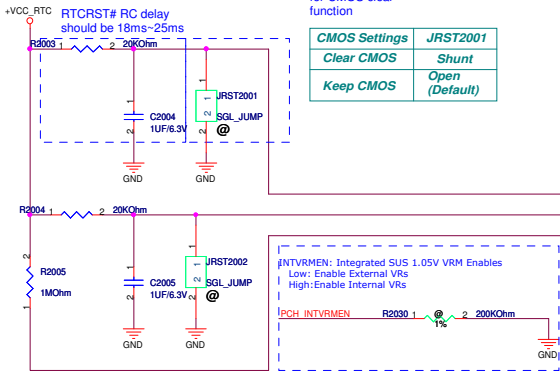
PEGATRON		Title : VID Controller	
PEGATRON COMPUTER INC		Engineer: Wing Cheng	
Size	Project Name		Rev
C	BA52HR/CR		1.0
Date: Friday, February 03, 2012		Sheet	19 of 94

RTC battery



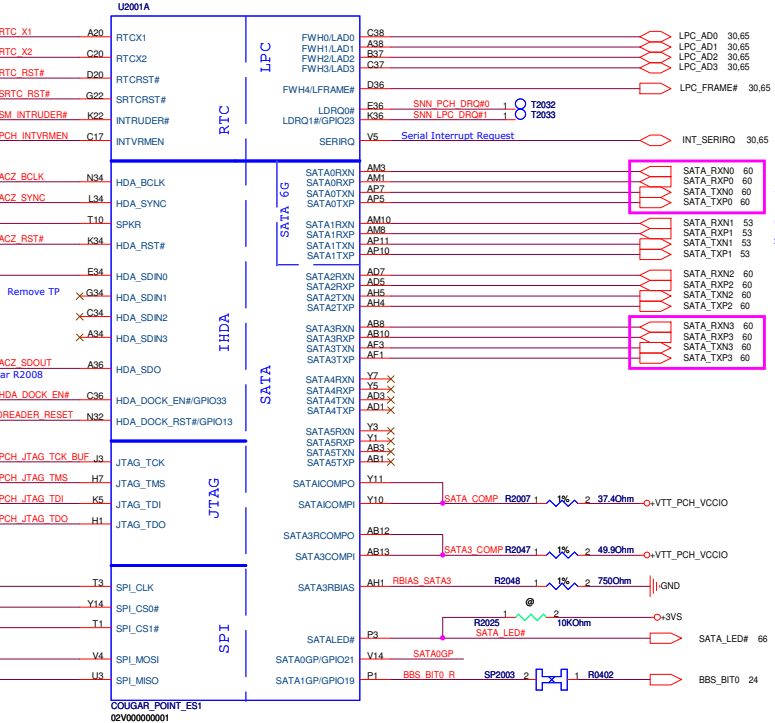
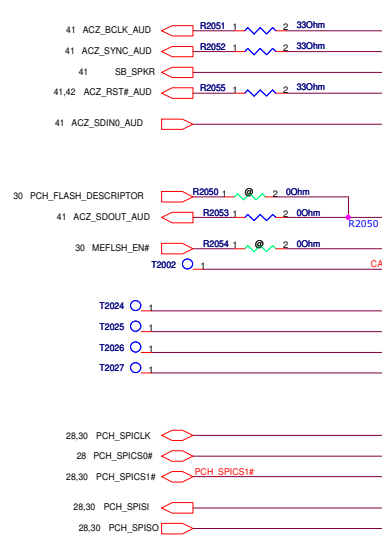
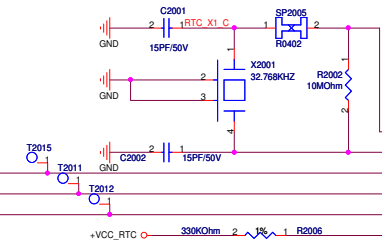
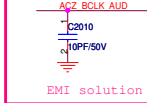
Request by CSC
for CMOS clear
function

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

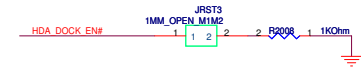


TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

INTVRMEN: Integrated SUS 1.05V VRM Enables
Low: Enable External VRs
High: Enable Internal VRs

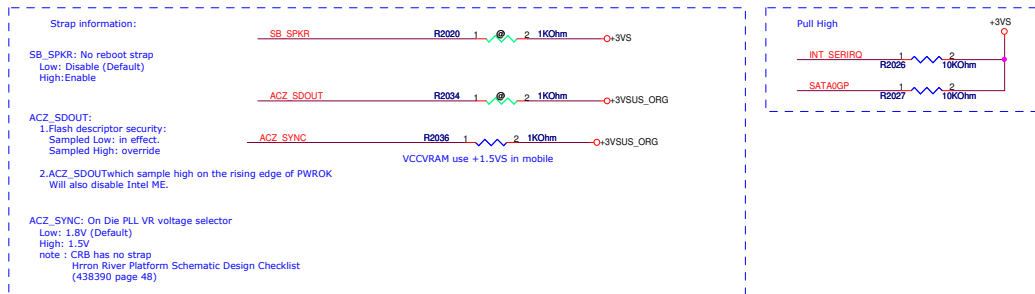


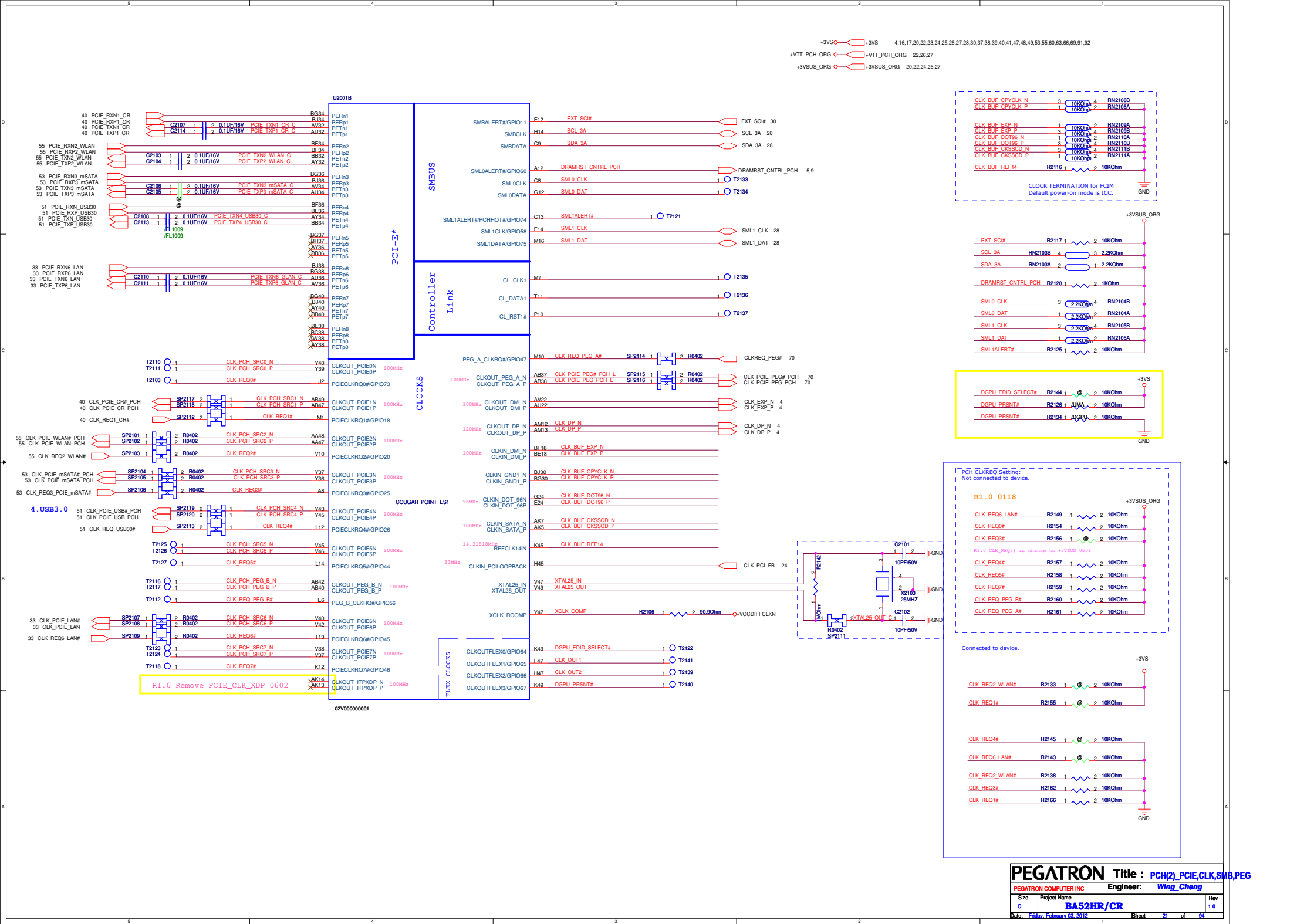
HDA_DKEN : Flash Descriptor Security Override
H = Disabled (Default)
L = Enabled
Note : Rising edge of PWROK

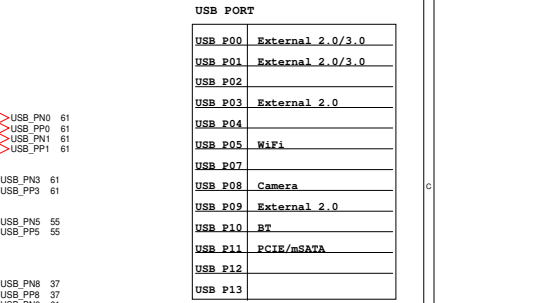
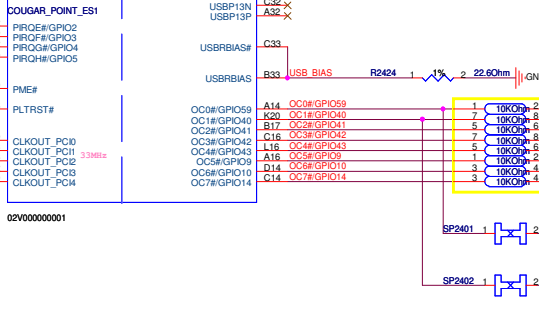
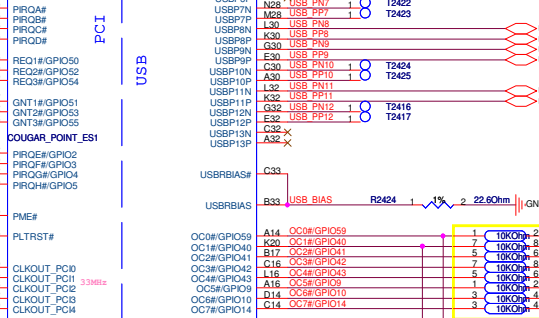
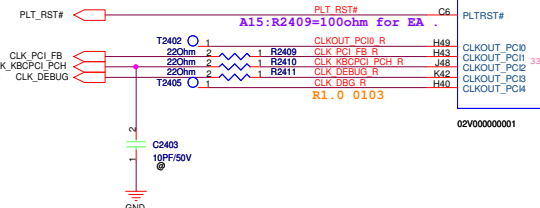
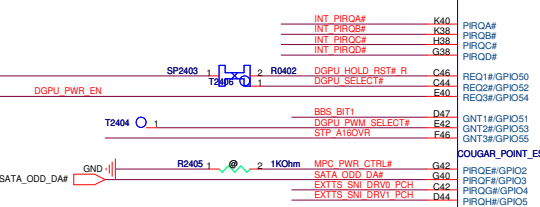


R1.0 add JRST3 to follow BIC50. Joyoung 0628

0200-00HU000 C.5 907552 A1 QMVY BGA942 INTEL/COUGAR POINT PCH



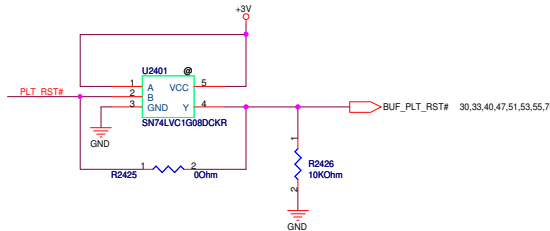
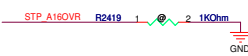




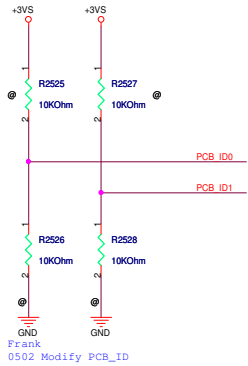
BBS_BIT0,BBS_BIT1 : Boot BIOS Strap

STP_A16OVR:
A16 swap override Strap/
Top-Block swap override jumper

Low=Enabled A16 swap override/ Top-Block swap override
High=Default



	PCB_ID1	PCB_ID0
A	L	L
B	L	H
C	H	L
MP		



R1.0

Add PCH_GPIO0_R.

Delete ICC_EN#.

Add PM_LANPHY_EN

Add HOST_ALERT#1_R.

Add SATA_DET#4_R.
DGPU_PWROK has 100 ms software delay,
no hardware delay requirement

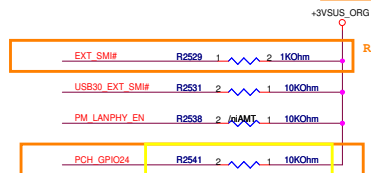
Reserve PCH_GPIO24

Add PLL_ODVR_EN.

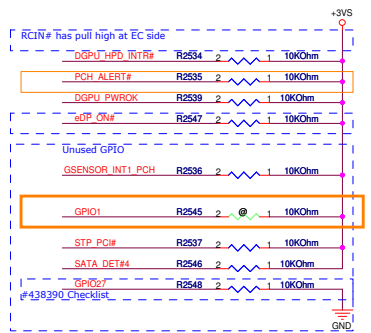
Add PSATA_PWR_EN#1_R.

Add SATA_ODD_PRST#_R and
FDI_OVRVLTG.

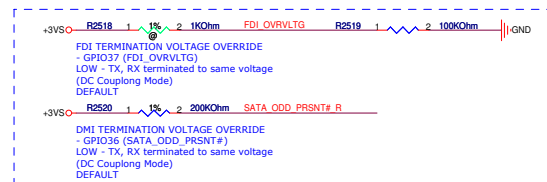
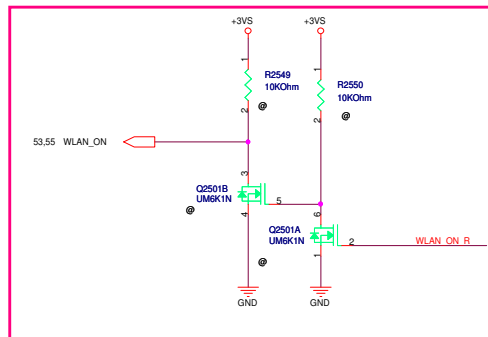
Add CRIT_TEMP_REP#_R.



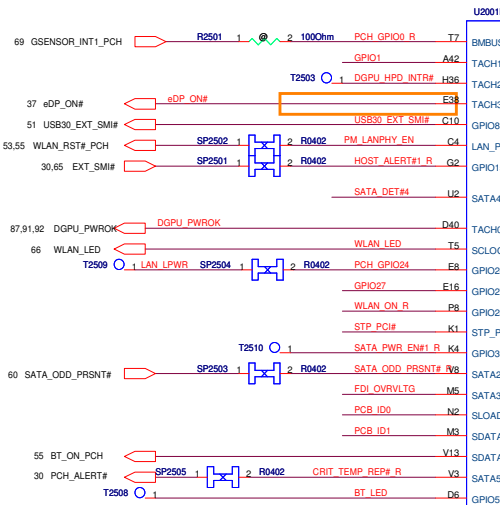
R1.0 mount R2541 for LAN_LPW 0615



R1.0 REMOVE DGPU_PWROK schematic 0602



R1.0 Change net name for single net. Joyoung (052)



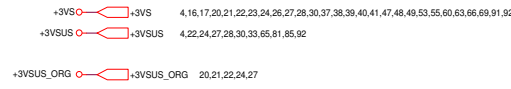
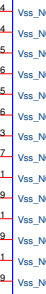
U2001F

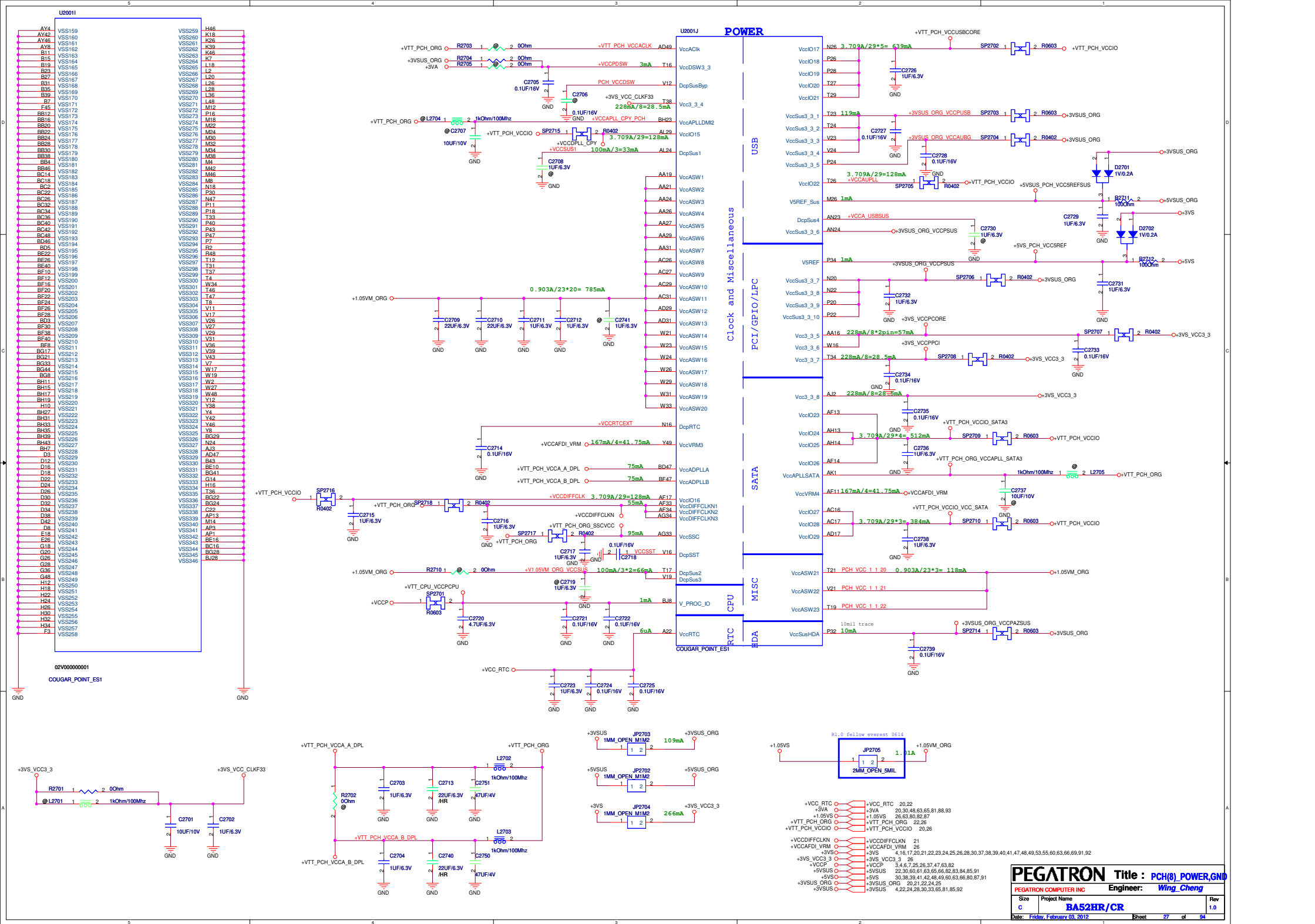


GPIO

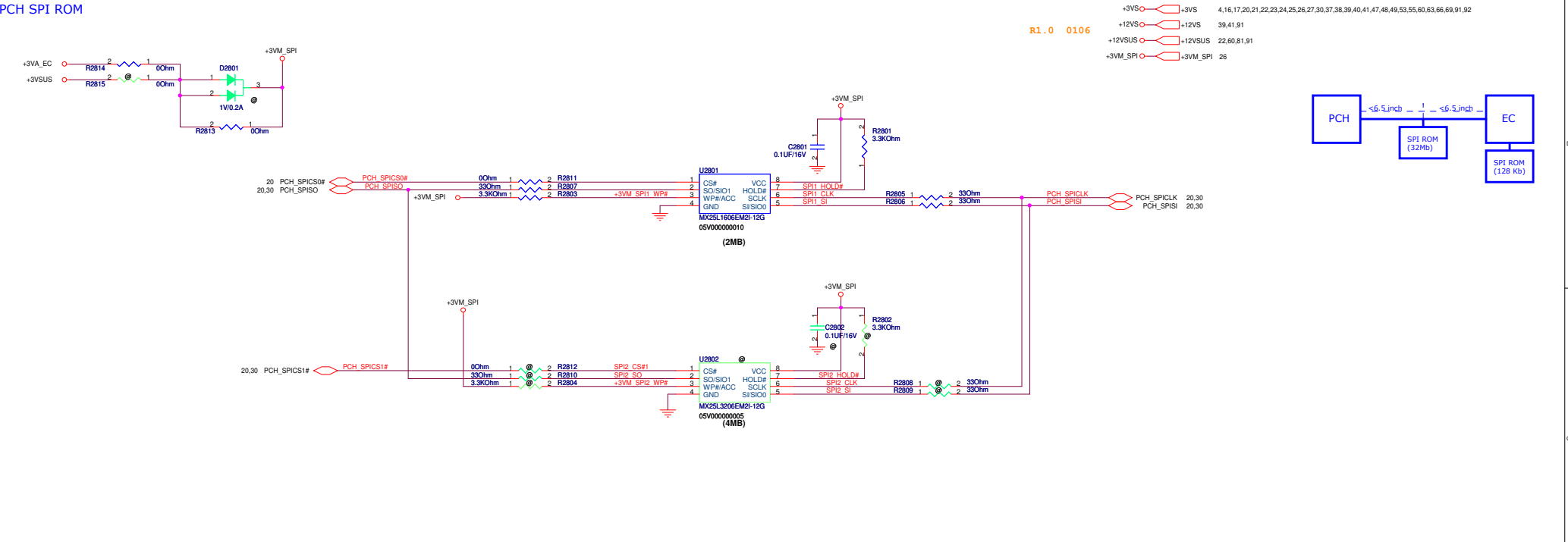
CPU/MISC

NCIF





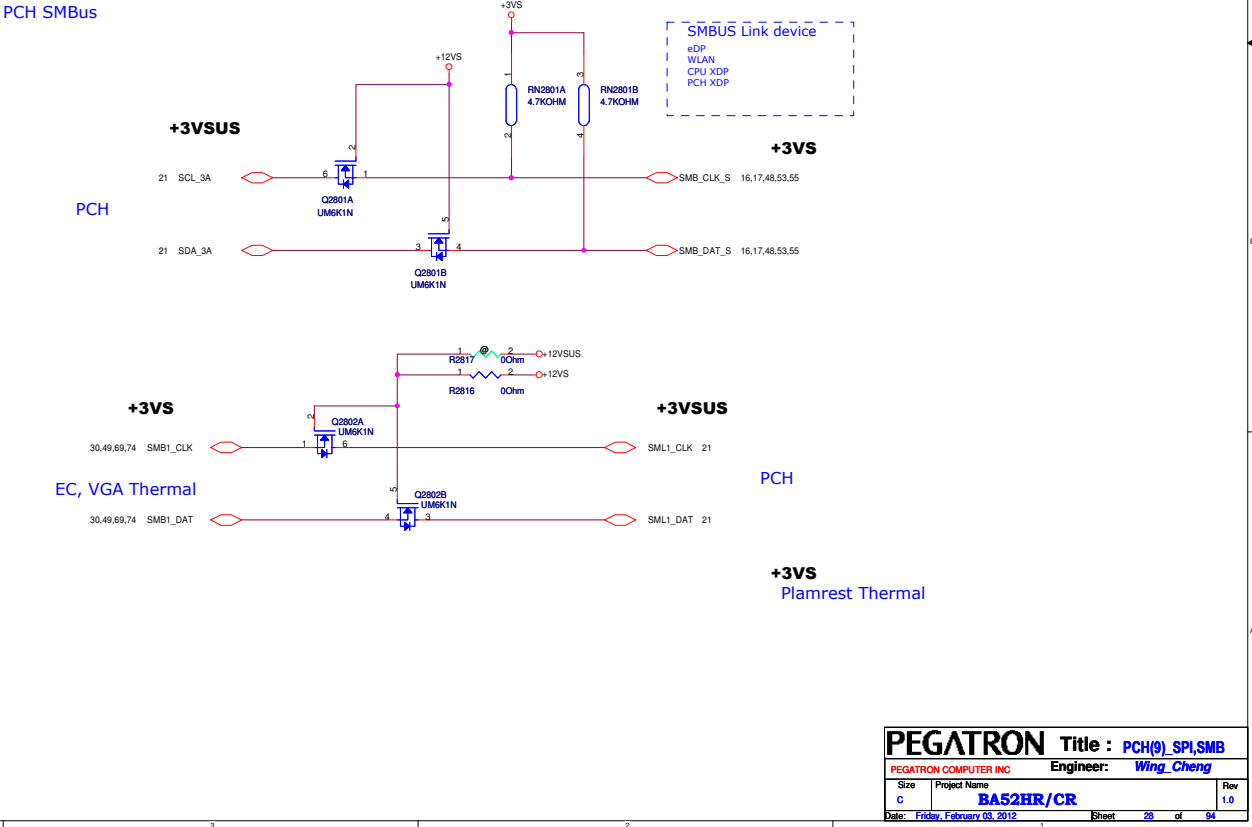
PCH SPI ROM

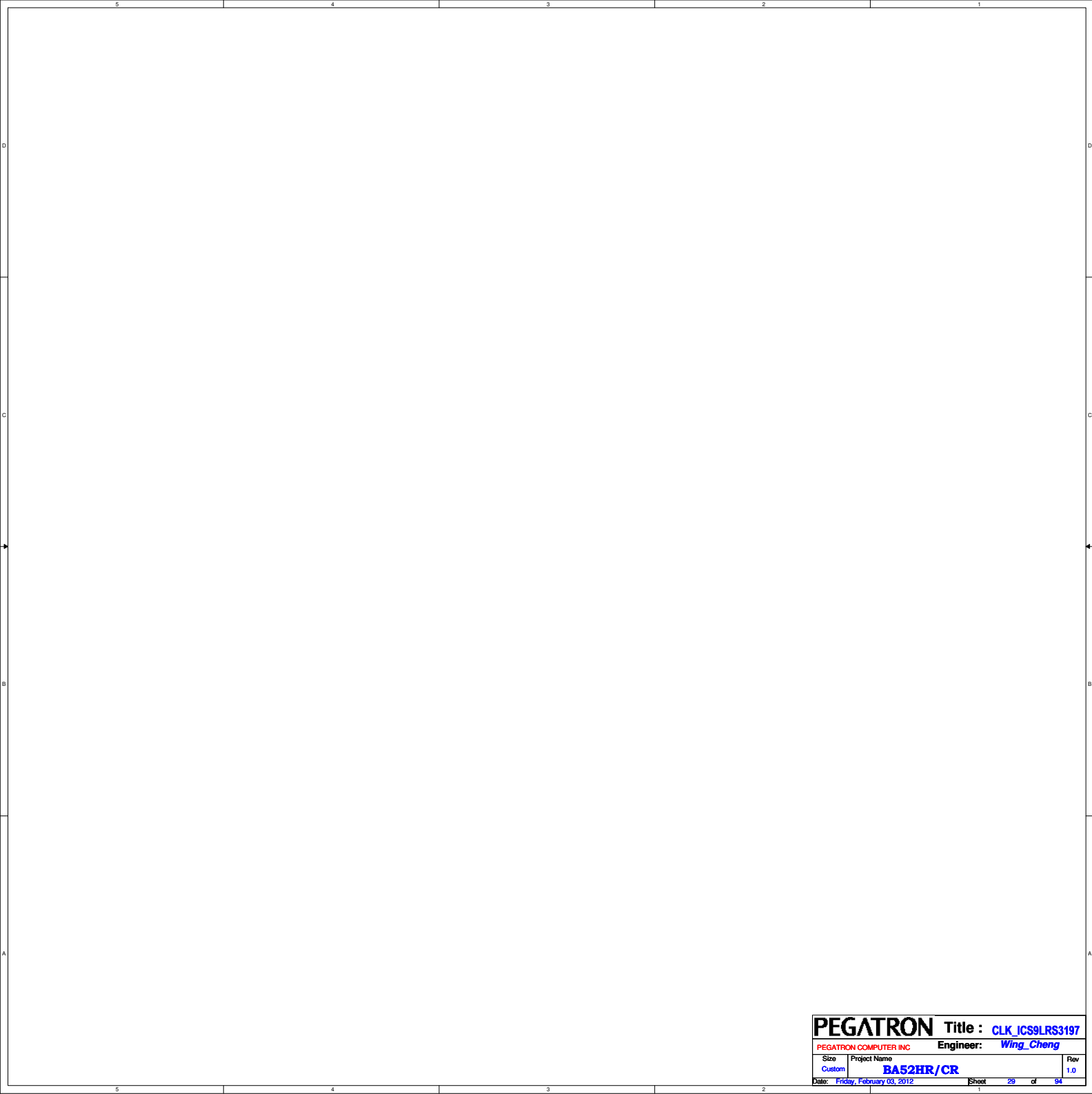


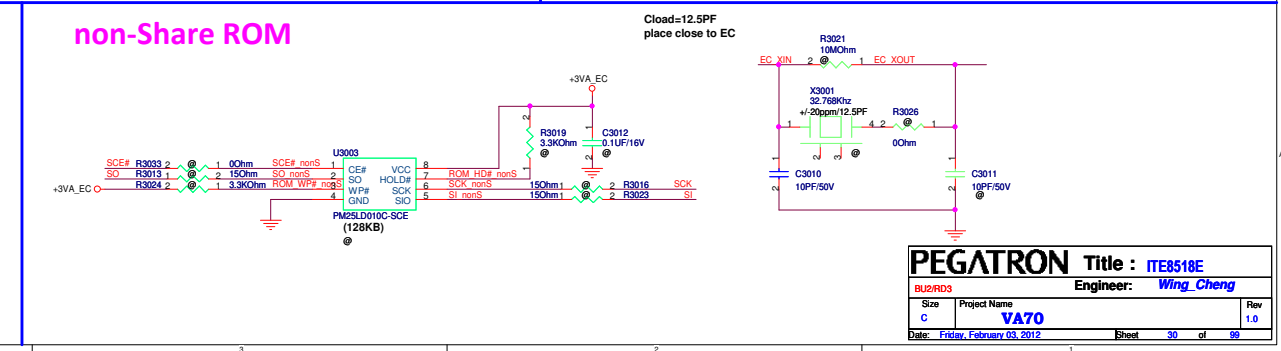
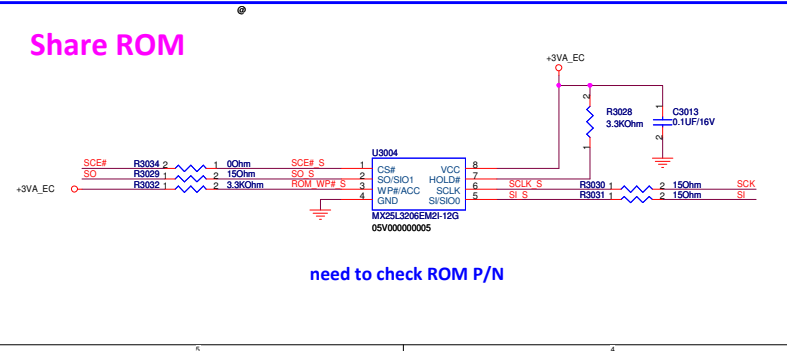
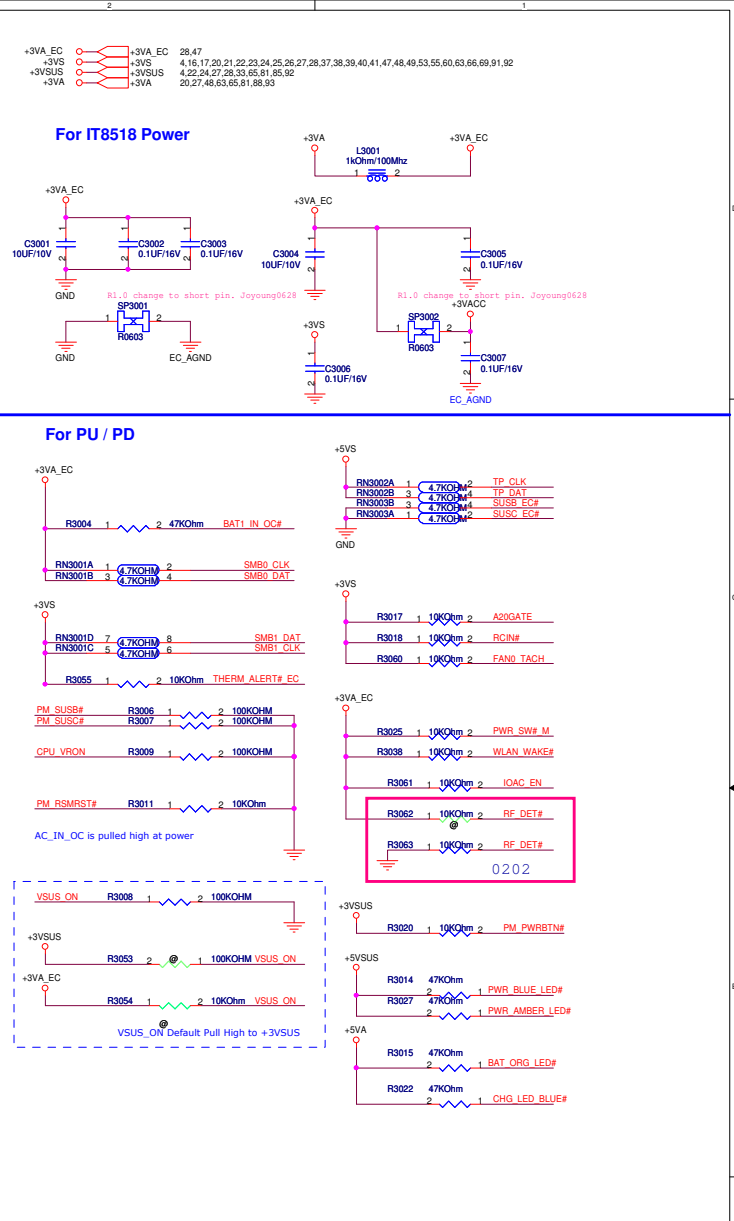
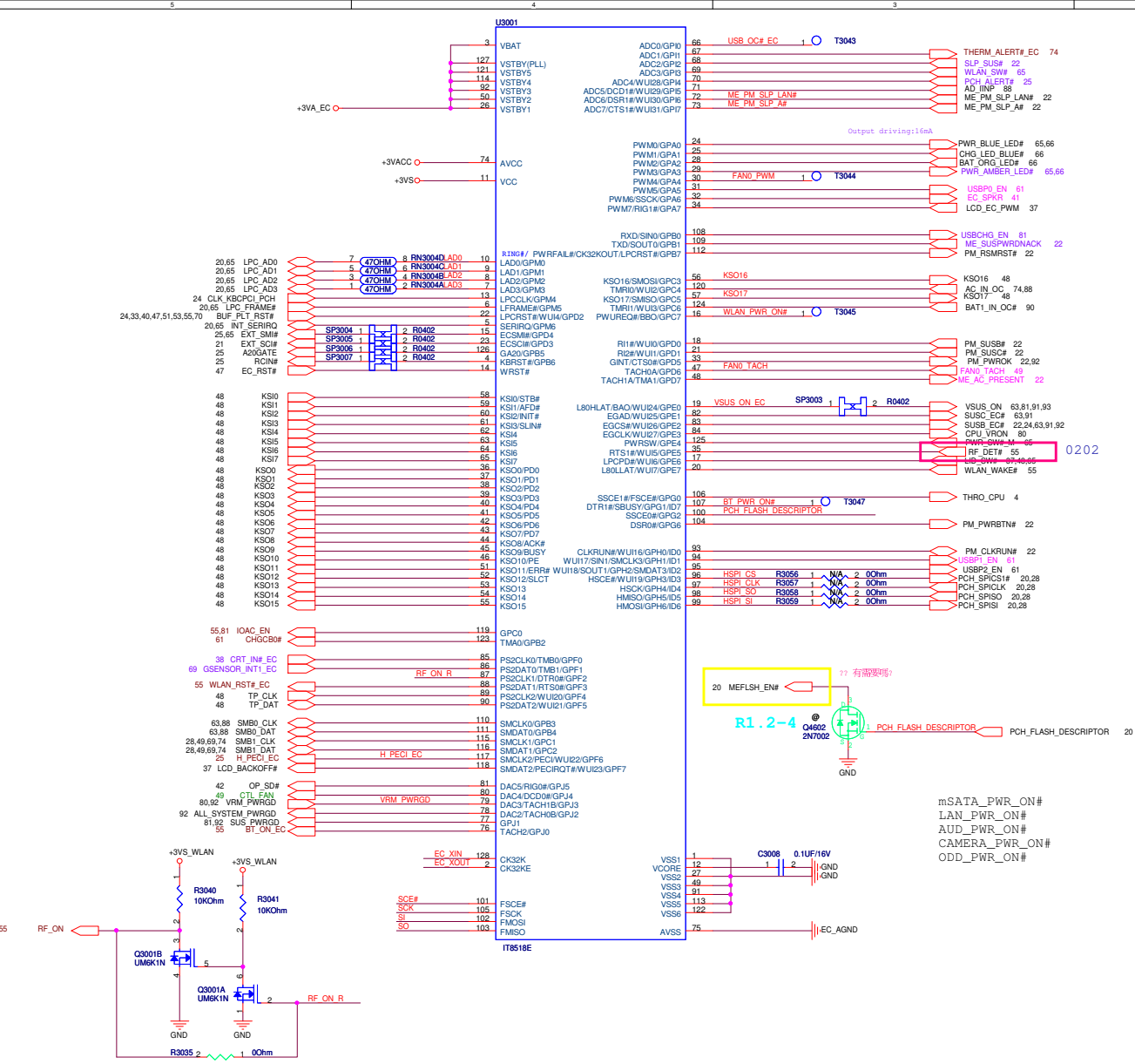
SPI Debug Connector



PCH SMBus







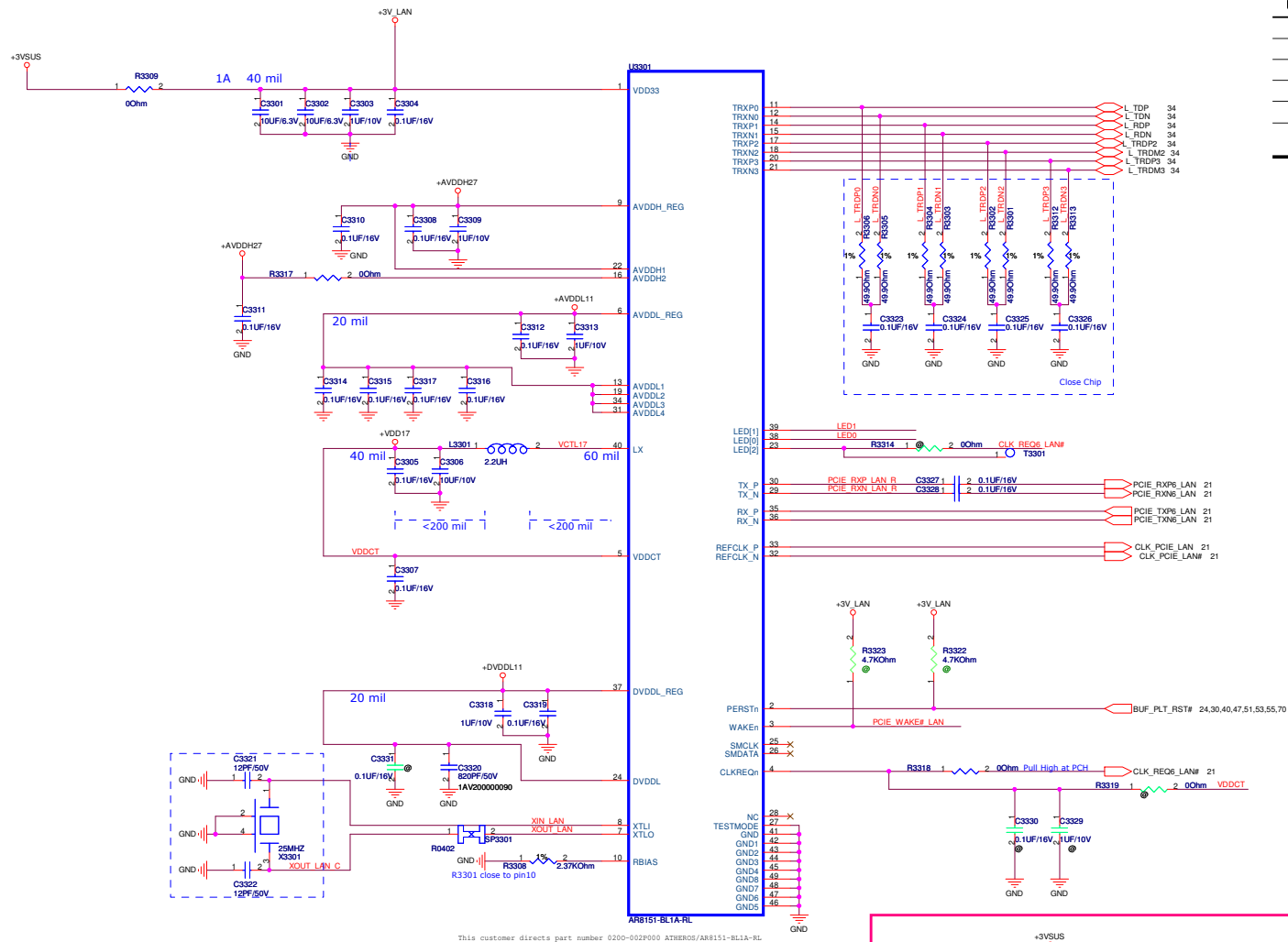
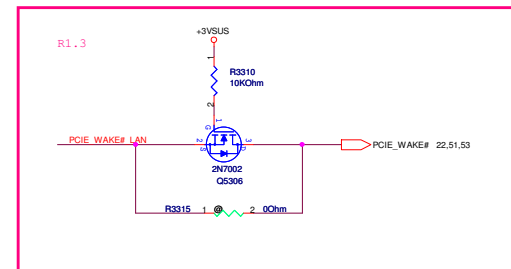
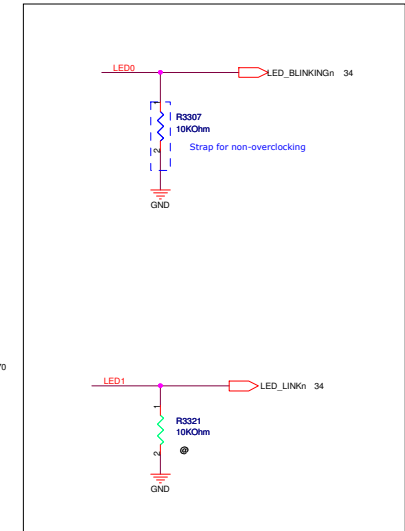
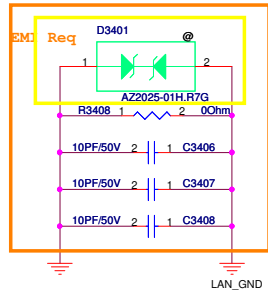
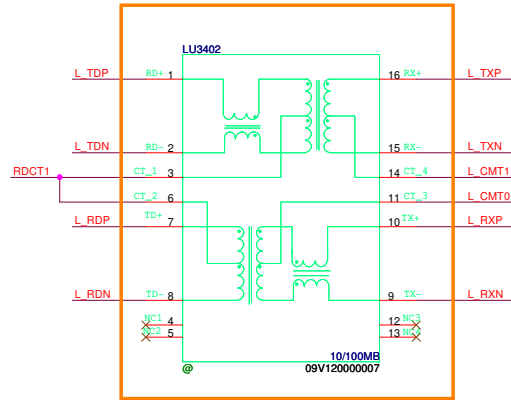


Table 2-6. LED Link Table

LED[0] LED_ACT	LED[1] LED_LINK	LED[2] LED_LINK_1000	Selected Speed	Link Status
High	High	High	Any Speed	Link Down
Blink	High	High	10 Mbps; Half-Duplex	Link Up
Blink	Low	High	10 Mbps; Full-Duplex	Link Up
Blink	Low	High	100 Mbps; Half-Duplex	Link Up
Blink	Low	High	100 Mbps; Full-Duplex	Link Up
Blink	Low	Low	Auto, 1000 Mbps, Full-Duplex	Link Up

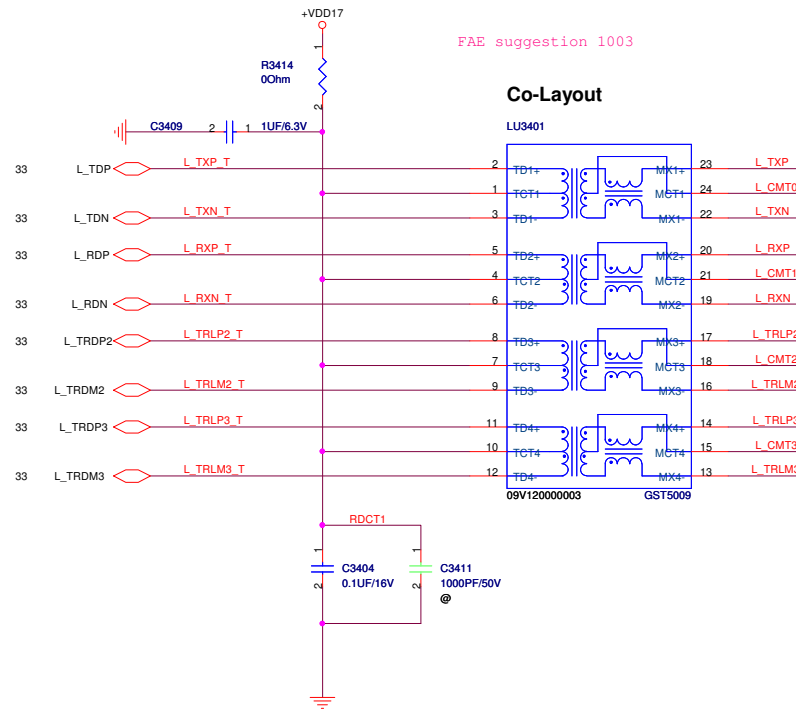


11/30 Swap for LU3401/LU3402 co-lay(Elmer)

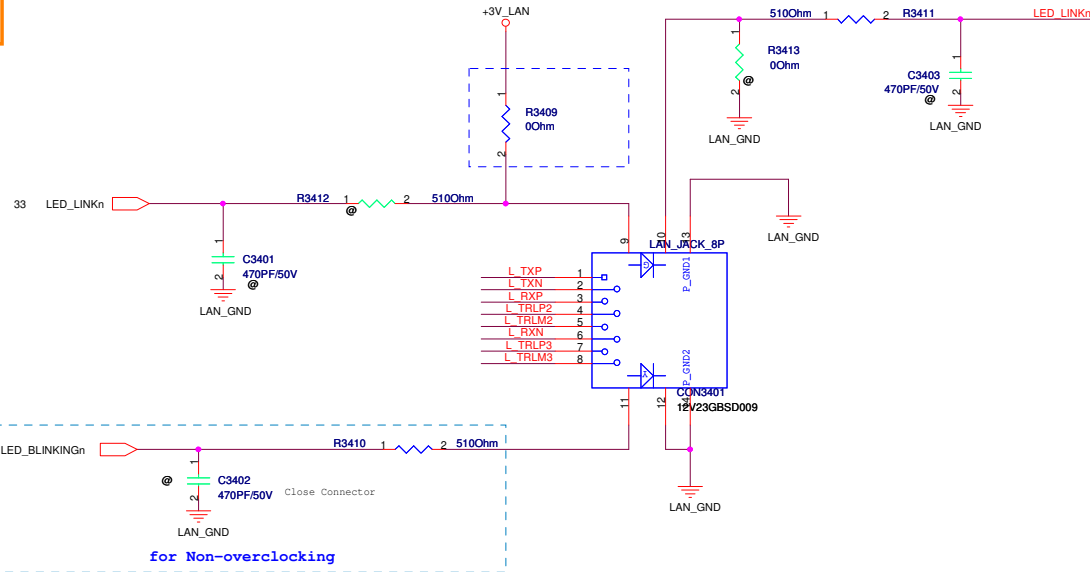
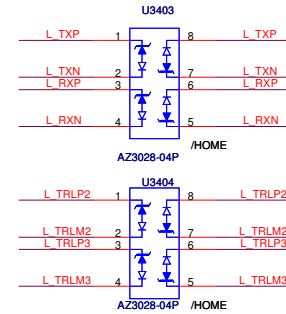
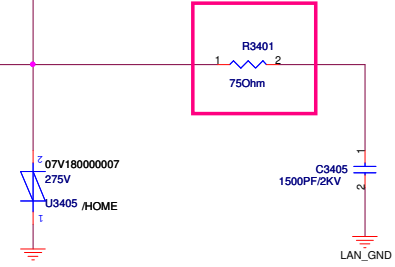


FAE suggestion 1003

Co-Layout



EMI suggest to change 0805 size 0921



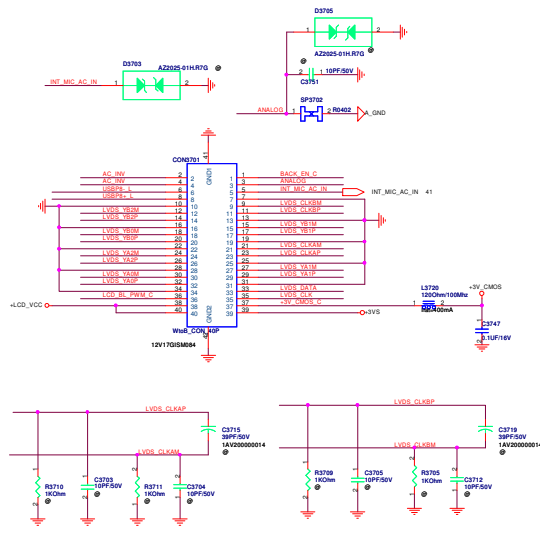
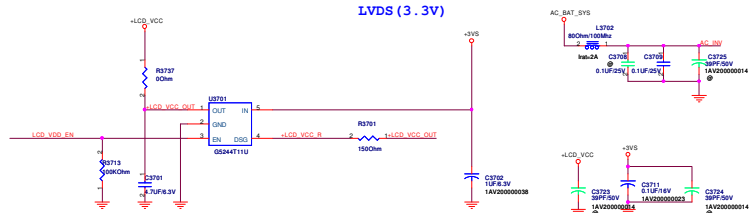
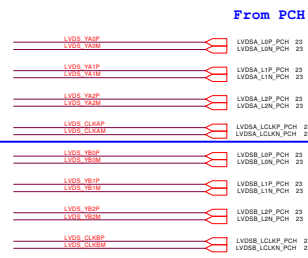
<Variant Name>

PEGATRON Title : RJ45/RJ11	
BG1-CSC-HW R&D Dept.5 Engineer: Ahren_chen	
Size Custom	Project Name PLFG
Date: Friday, February 03, 2012	Sheet 34 of 99

LVDS

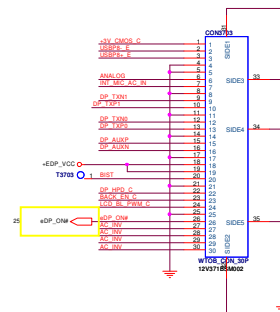
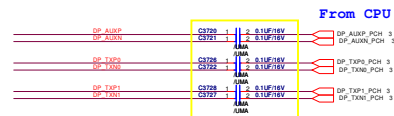
CH A

CH B



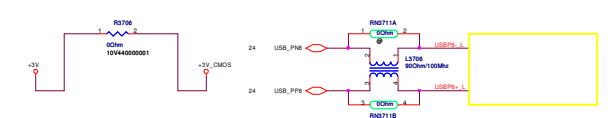
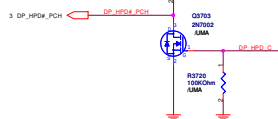
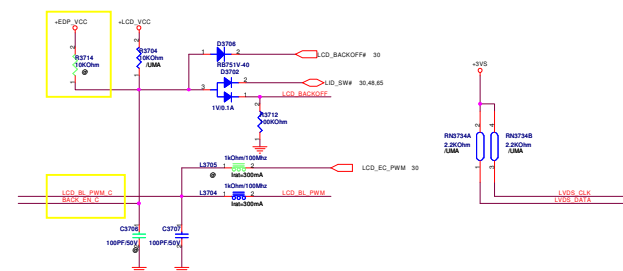
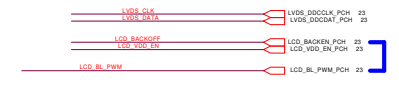
eDP

eDP (3V)



LVDS/EDP共用pin

LVDS/EDP共用pin



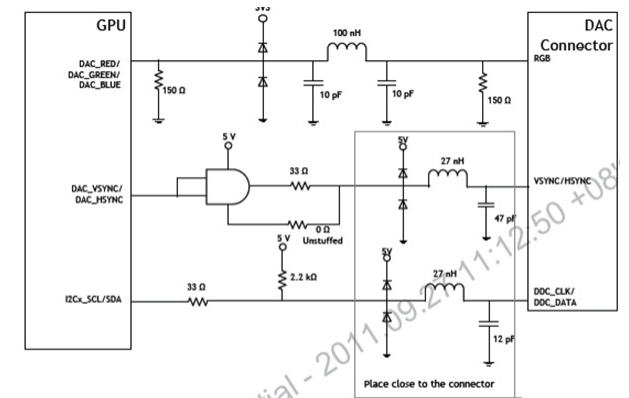
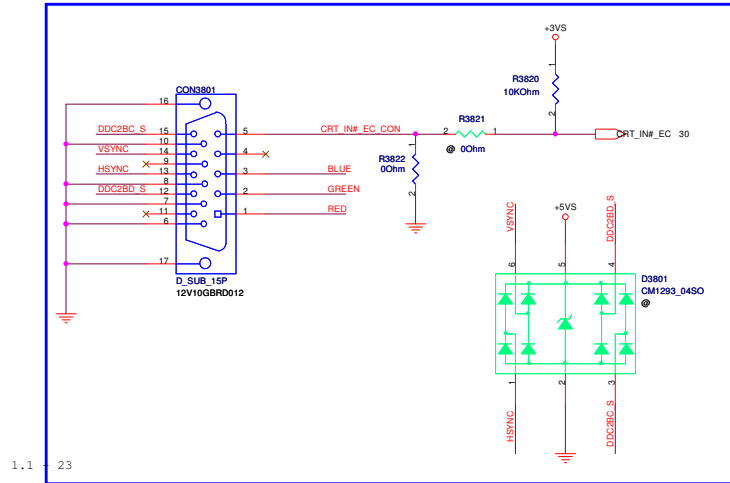
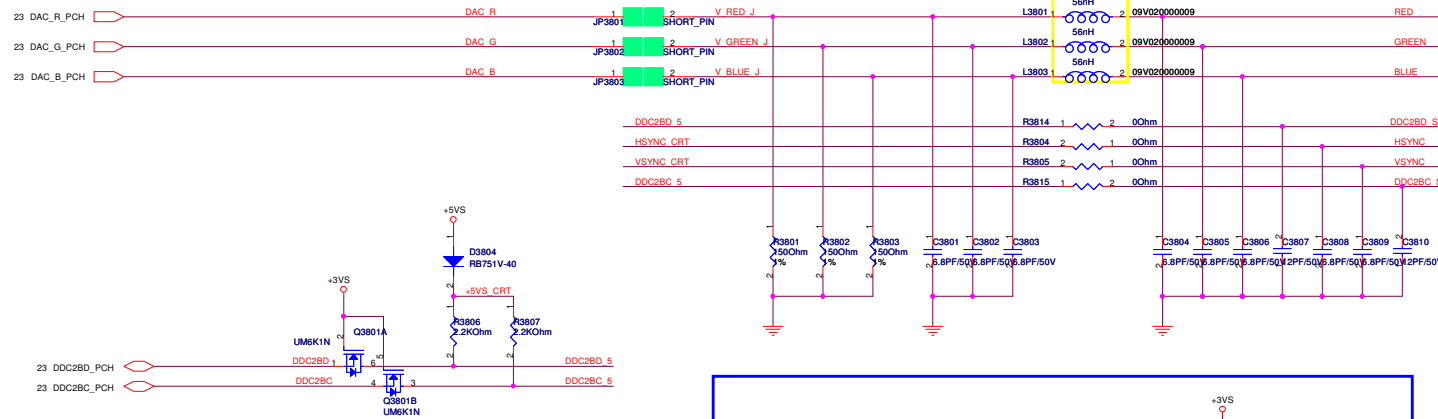
RN3733 close to EDP connector(CON3703)

LVDS connector(CON3701)

EDP connector(CON3703)



Check UMA and DSC inductor value



RSET Requirements: DACA_RSET= 124Ω, 1%, stuffed by default.

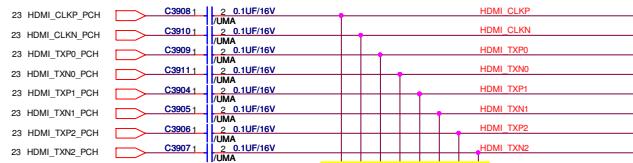
Figure 71. GPU-DAC Connections

The LC filter circuit (NV DSC only)

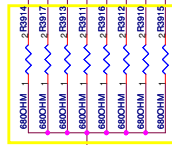
DDC: L=27nH, C=12PF

HSYNC/VSYNC: L=27nH, C=47PF

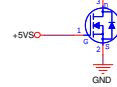
RGB: L=100nH, C=10PF



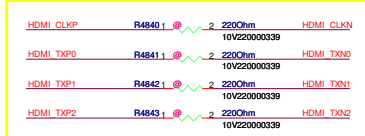
Close to connector and do T routing



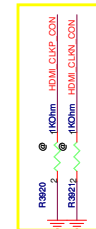
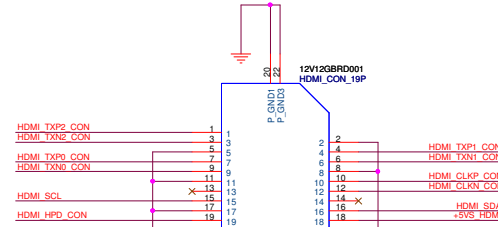
R3910, R3911, R3912, R3913, R3914, R3915, R3916, R3917
Intel design guide : 680ohm /UMA
NV reference schematics : 499ohm /DGPUO



EMI solution

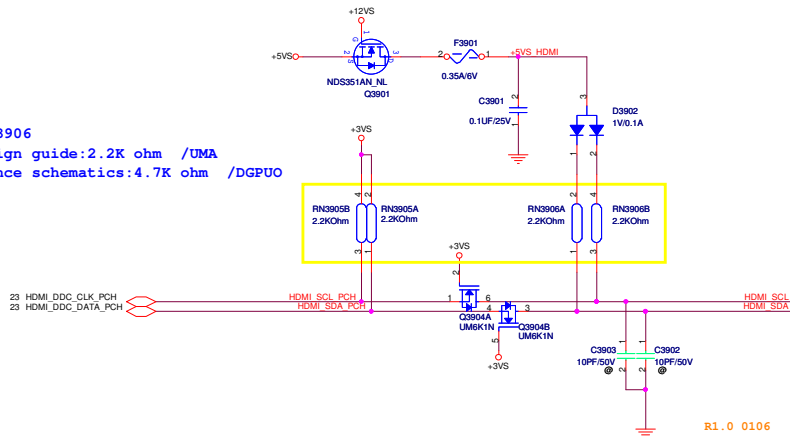


HDMI_SCL & HDMI_SDA : no via , trace length should be as short as possible

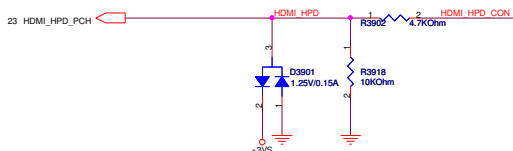


EMI solution

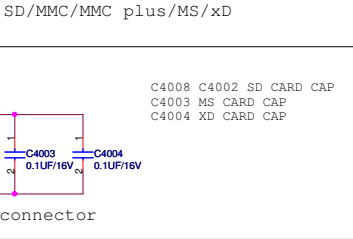
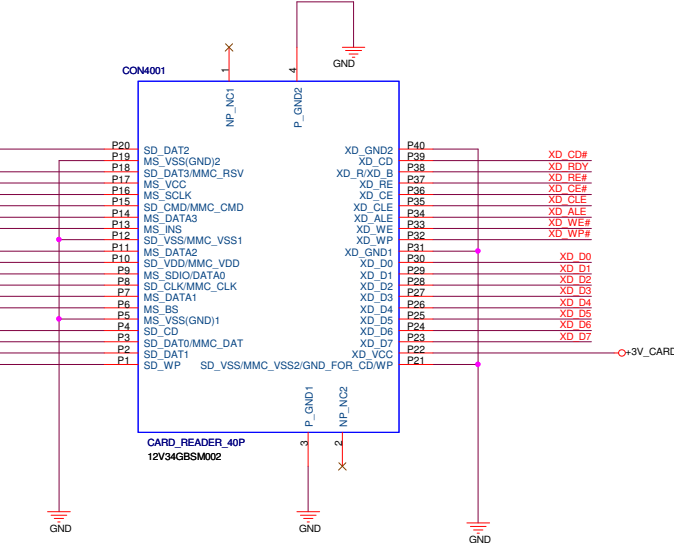
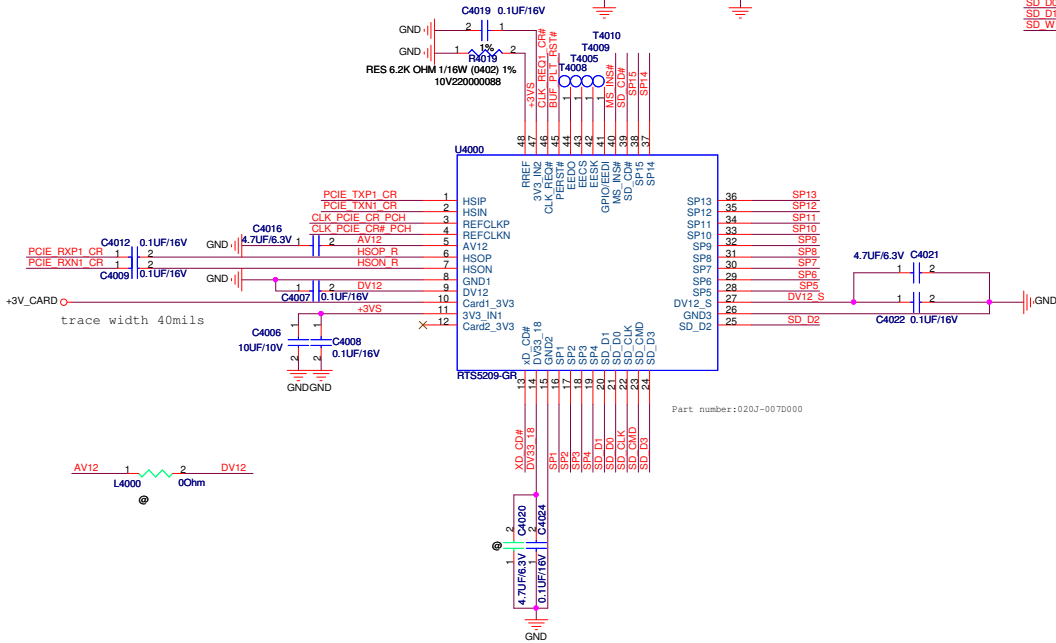
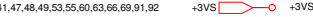
RN3905, RN3906
Intel design guide: 2.2K ohm /UMA
NV reference schematics: 4.7K ohm /DGPUO



R1.0 0106
HDMI HPD Cost Reduced Level Shifter Design Recommendation



From System's PCIE interface



Pin Name	Description
SP1	SD_D7/XD_RDY
SP2	SD_D6/XD_RE#
SP3	SD_D5/XD_CE#
SP4	SD_D4/XD_WE#
SP5	MS_BS/XD_CLE
SP6	MS_D5/XD_ALE
SP7	MS_D1/XD_WP#
SP8	MS_D4/XD_D0
SP9	MS_D0/XD_D1
SP10	MS_D2/XD_D2
SP11	MS_D6/XD_D3
SP12	MS_D3/XD_D4
SP13	MS_D7/XD_D5
SP14	MS_CLK/XD_D6
SP15	SD_WP/XD_D7

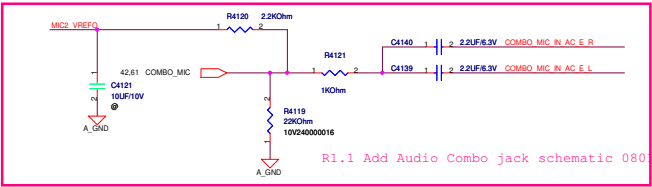
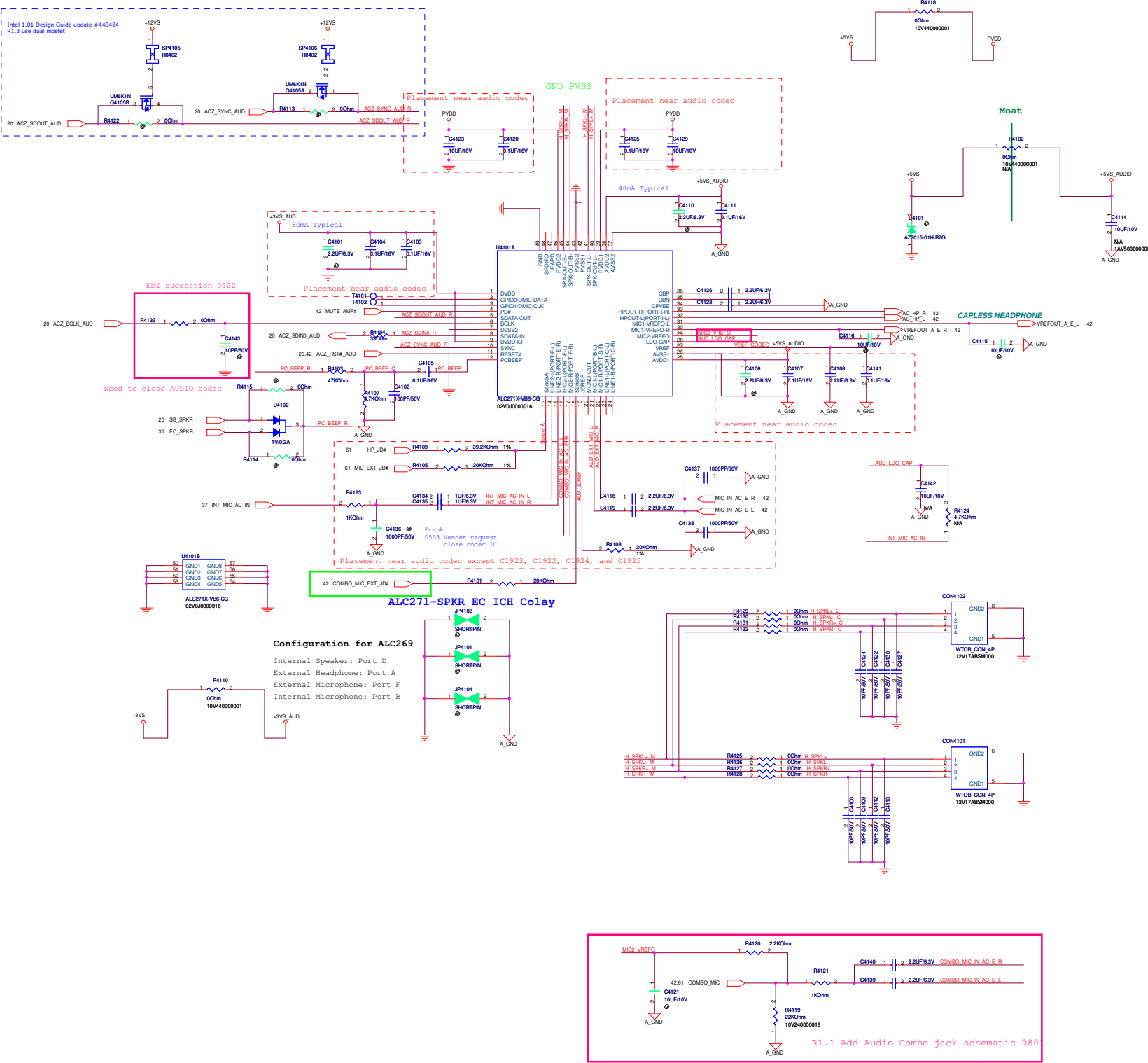
SP1	SD_D7	XD_RDY
SP2	SD_D6	XD_RE#
SP3	SD_D5	XD_CE#
SP4	SD_D4	XD_WE#
SP5	MS_BS	XD_CLE
SP6	MS_D5	XD_ALE
SP7	MS_D1	XD_WP#
SP8	MS_D4	XD_D0
SP9	MS_D0	XD_D1
SP10	MS_D2	XD_D2
SP11	MS_D6	XD_D3
SP12	MS_D3	XD_D4
SP13	MS_D7	XD_D5
SP14	MS_CLK	XD_D6
SP15	SD_WP	XD_D7

Remove Serial Flash

Reserve for BIOS boot function

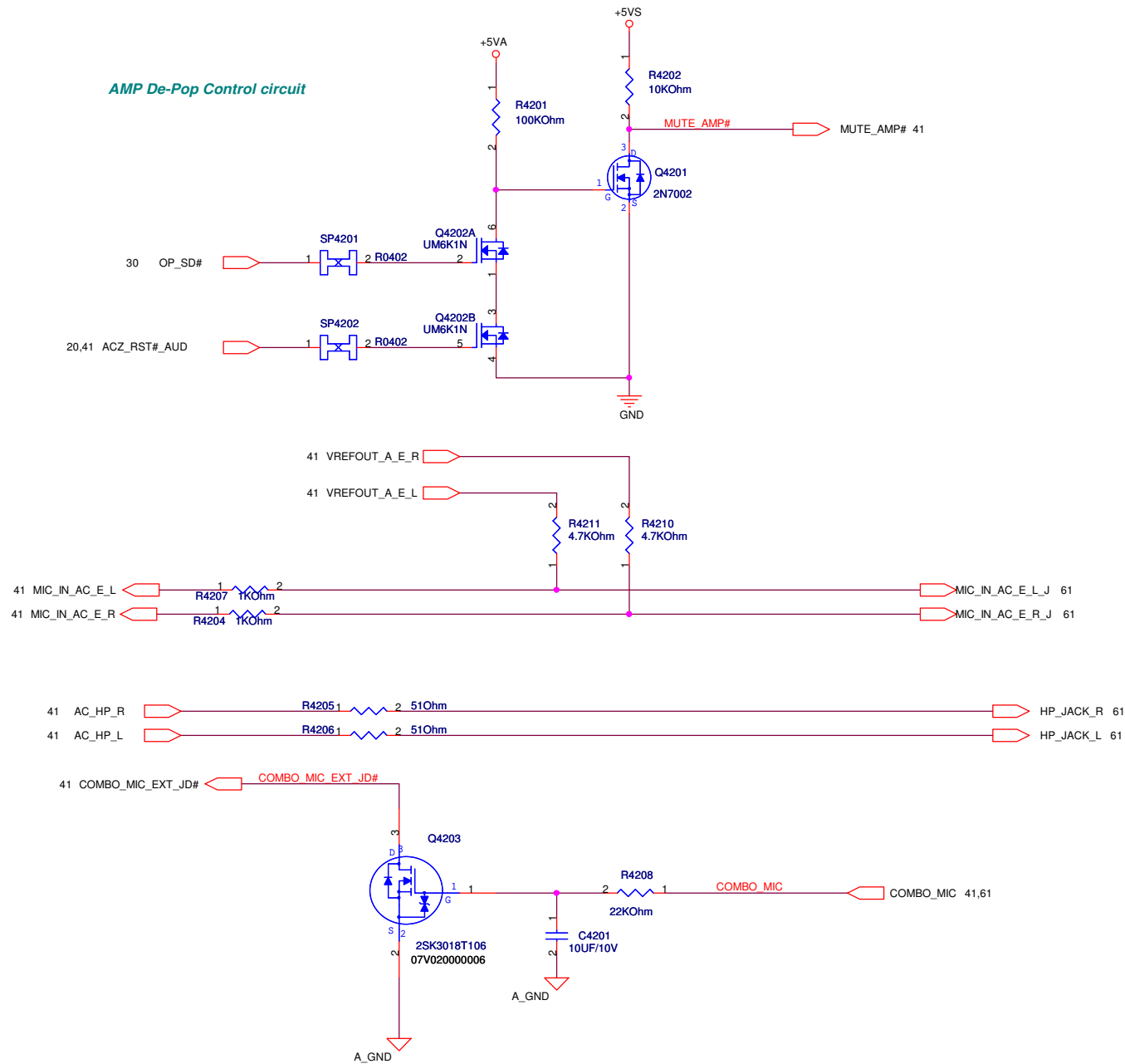
When EECS switch to be D3-Delink sideband signal, Serial Flash function is disabled.

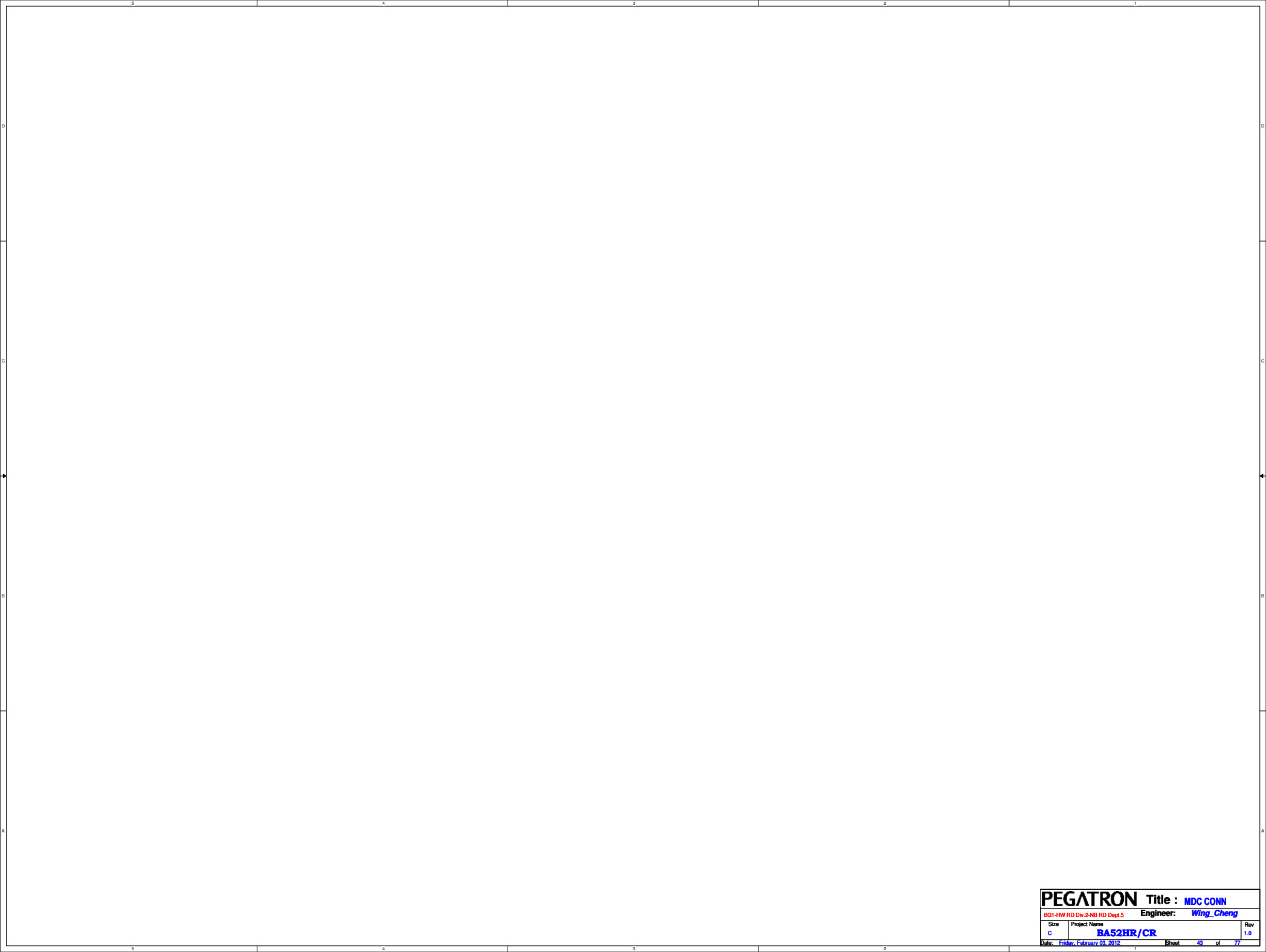
Share Pin



R1.1 Add Audio Combo jack schematic 080

AMP De-Pop Control circuit





PEGATRON		Title : MDC CONN	
BG1-HW RD Dw.2-NB RD Dept.5		Engineer: Wing_Cheng	
Size	Project Name		Rev
C	BA52HR/CR		1.0
Date: Friday, February 03, 2012		Sheet	43 of 77



Del Entry audio circuit

SR-8
0121-11

PEGATRON		Title : CODEC-ALC269	
ASUSTeK COMPUTER INC. NB1		Engineer: Wing_Cheng	
Size Custom	Project Name BA52HR/CR	Rev 1.0	
Date: Friday, February 03, 2012		Sheet 44 of 77	

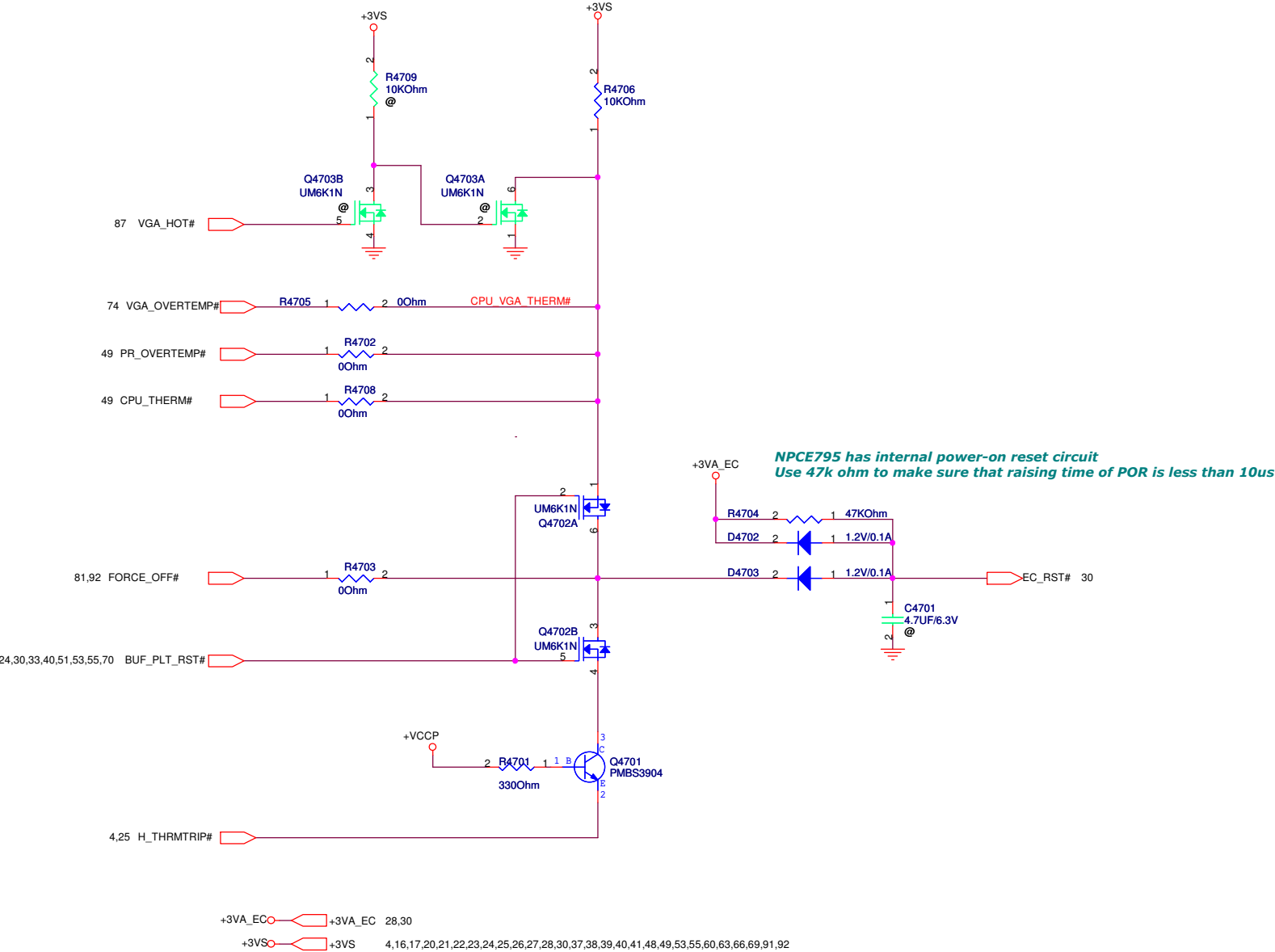


Del Entry audio circuit

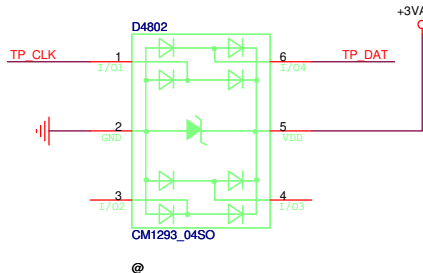
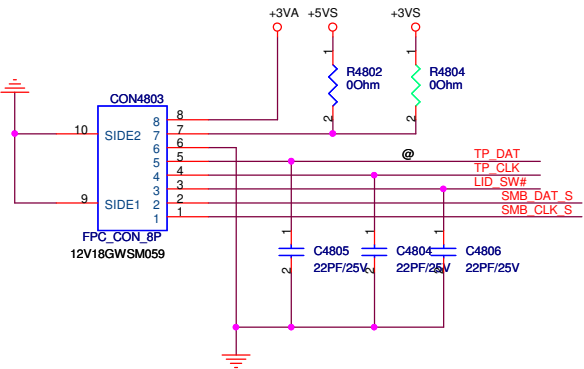
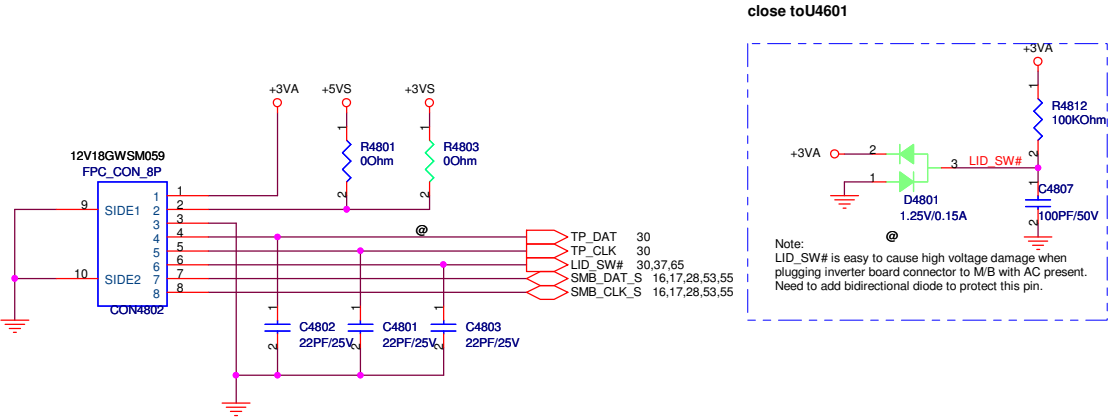
SR-8
0121-11

PEGATRON		Title : AUDIO ALC269	
BU1-RD Div.1+HW RD Dept.1		Engineer: Wing_Cheng	
Size Custom	Project Name BA52HR/CR	Rev 1.0	
Date: Friday, February 03, 2012		Sheet 45 of 77	

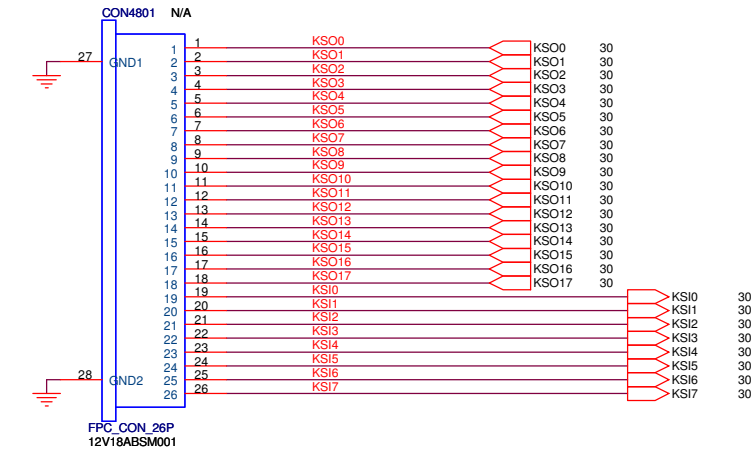
Thermal Policy



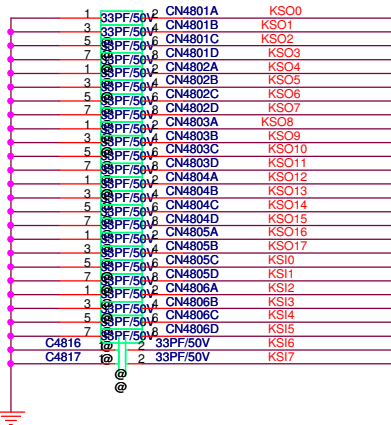
Touch Pad Button/ Hall Sensor



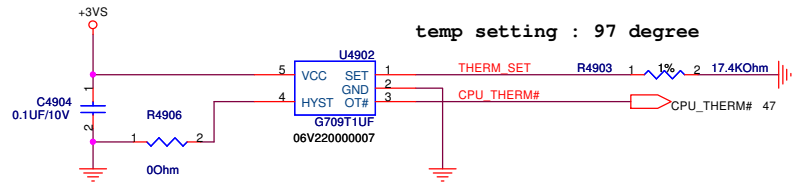
Keyboard



1218-00MW000

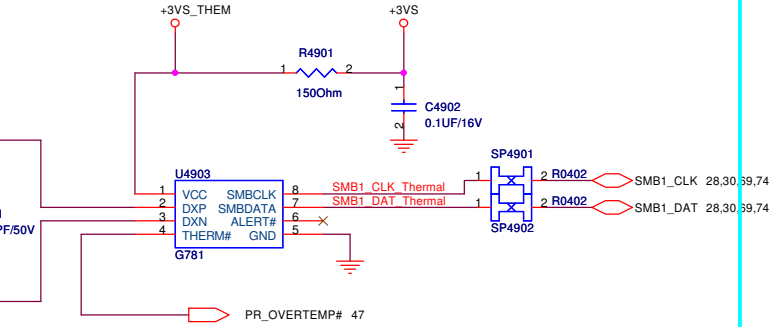
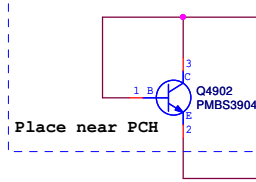


U5001 Close to CPU



Plam Rest Thermal Sensor

PHILIP PMBS3904
Place in the center of Plamrest.



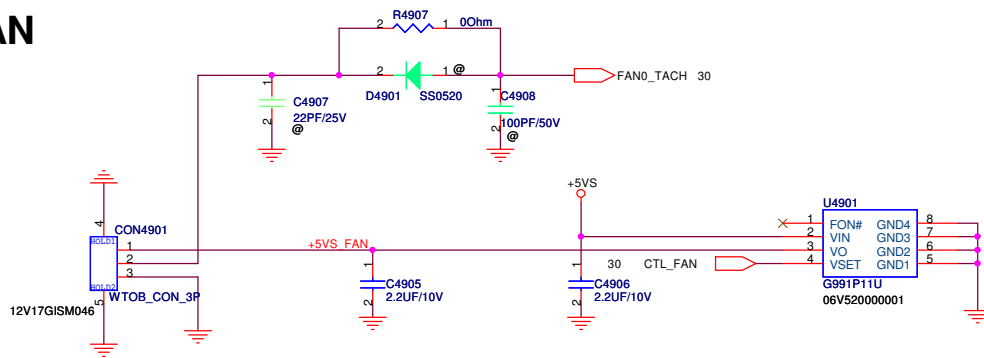
U4903 under palmrest

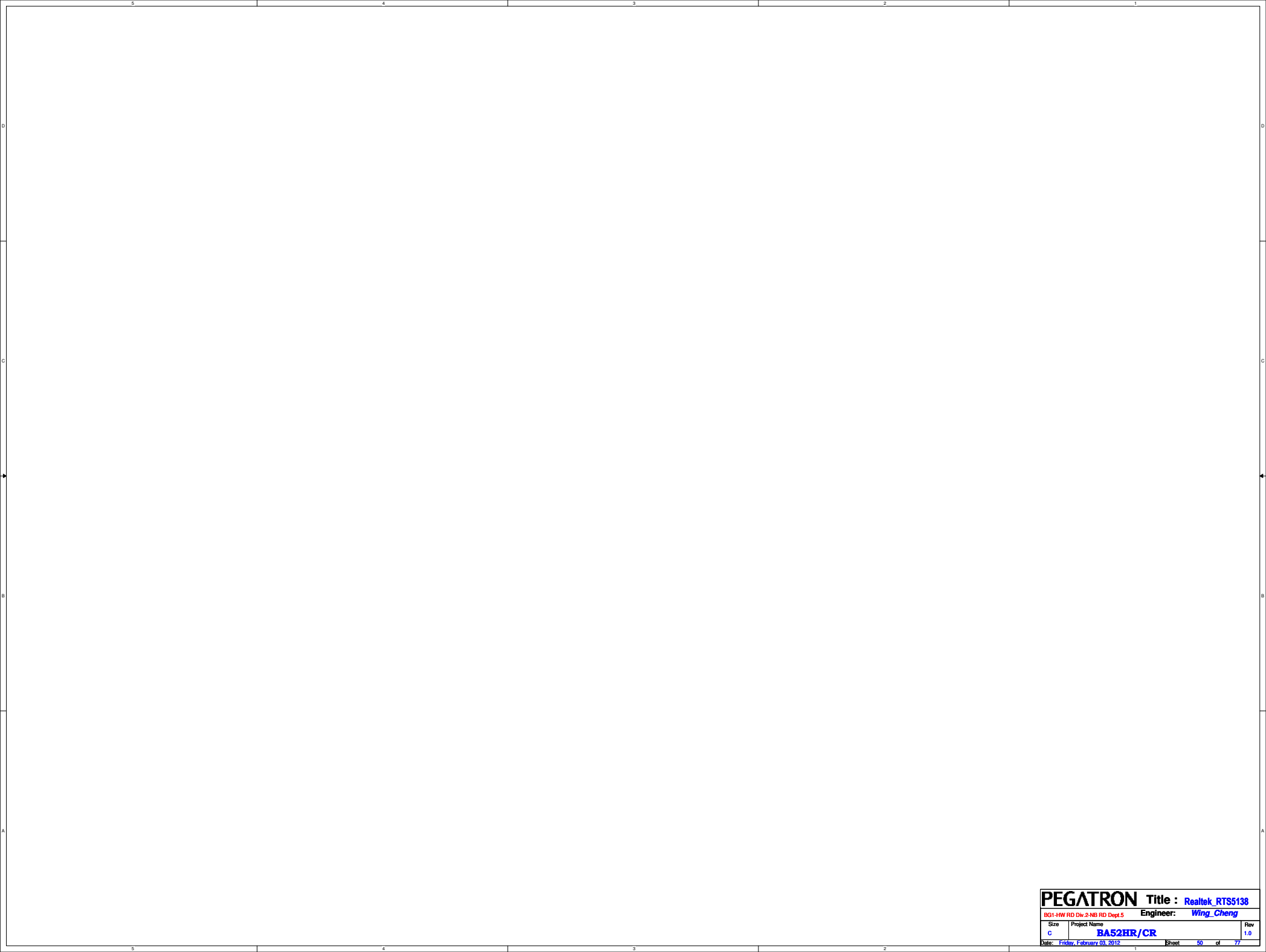
SMBUS addr=1001100x (98)

U4903: Remote(Local) thermal sensor,use remote mode.

R1.2-10

FAN





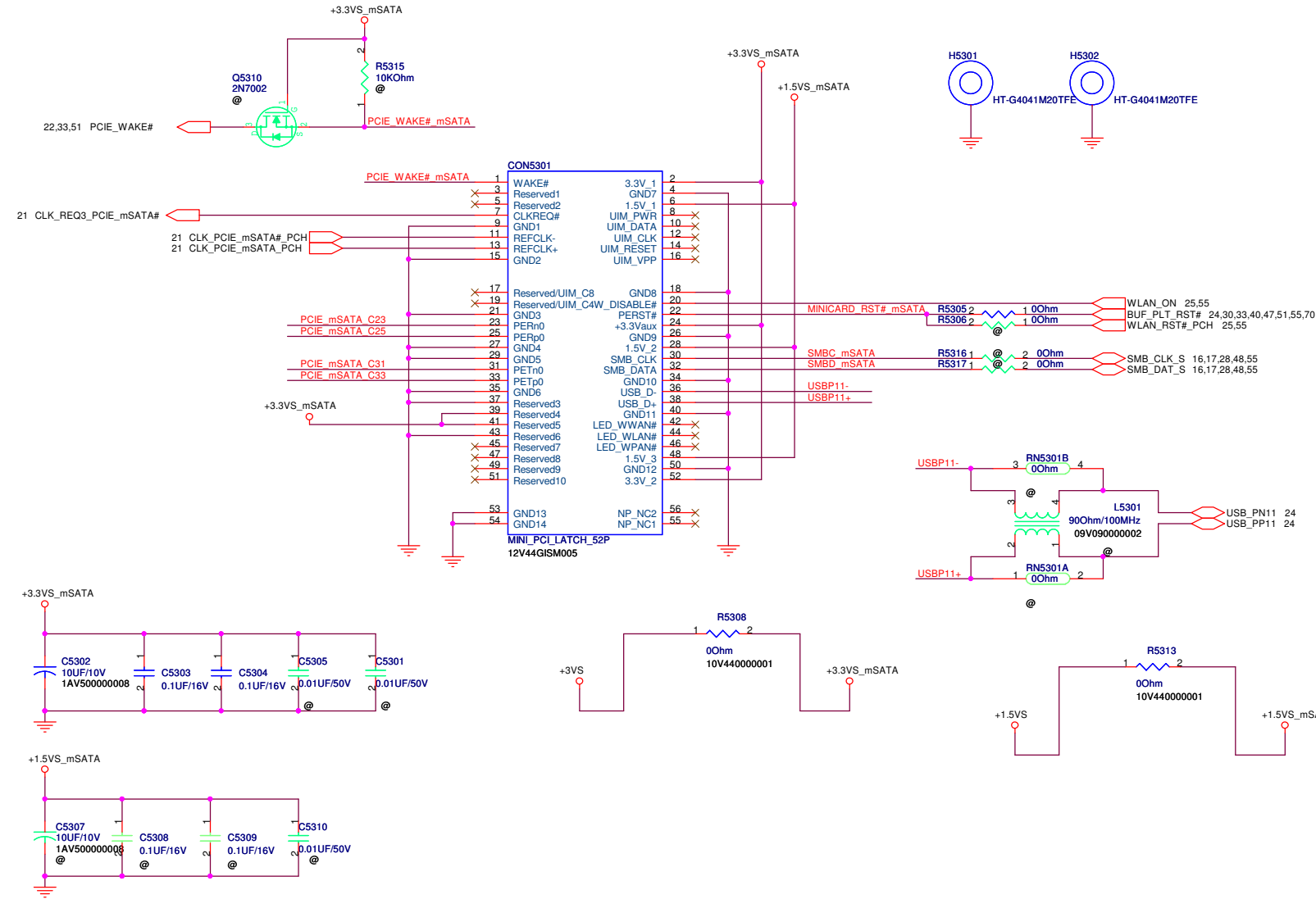
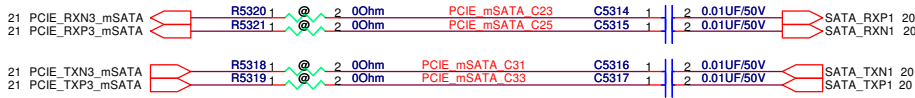
PEGATRON		Title : Realtek_RT55138	
BG1-HW RD Dw.2-NB RD Dept.5		Engineer: Wing_Cheng	
Size C	Project Name BA52HR/CR	Rev 1.0	
Date: Friday, February 03, 2012		Sheet 50 of 77	



PEGATRON		Title : PCIE NEW CARD	
BU1-RD Div.1-HW RD Dept.1		Engineer: <i>Wing_Cheng</i>	
Size Custom	Project Name BA52HR/CR		Rev 1.0
Date: Friday, February 03, 2012		Sheet 52 of 77	

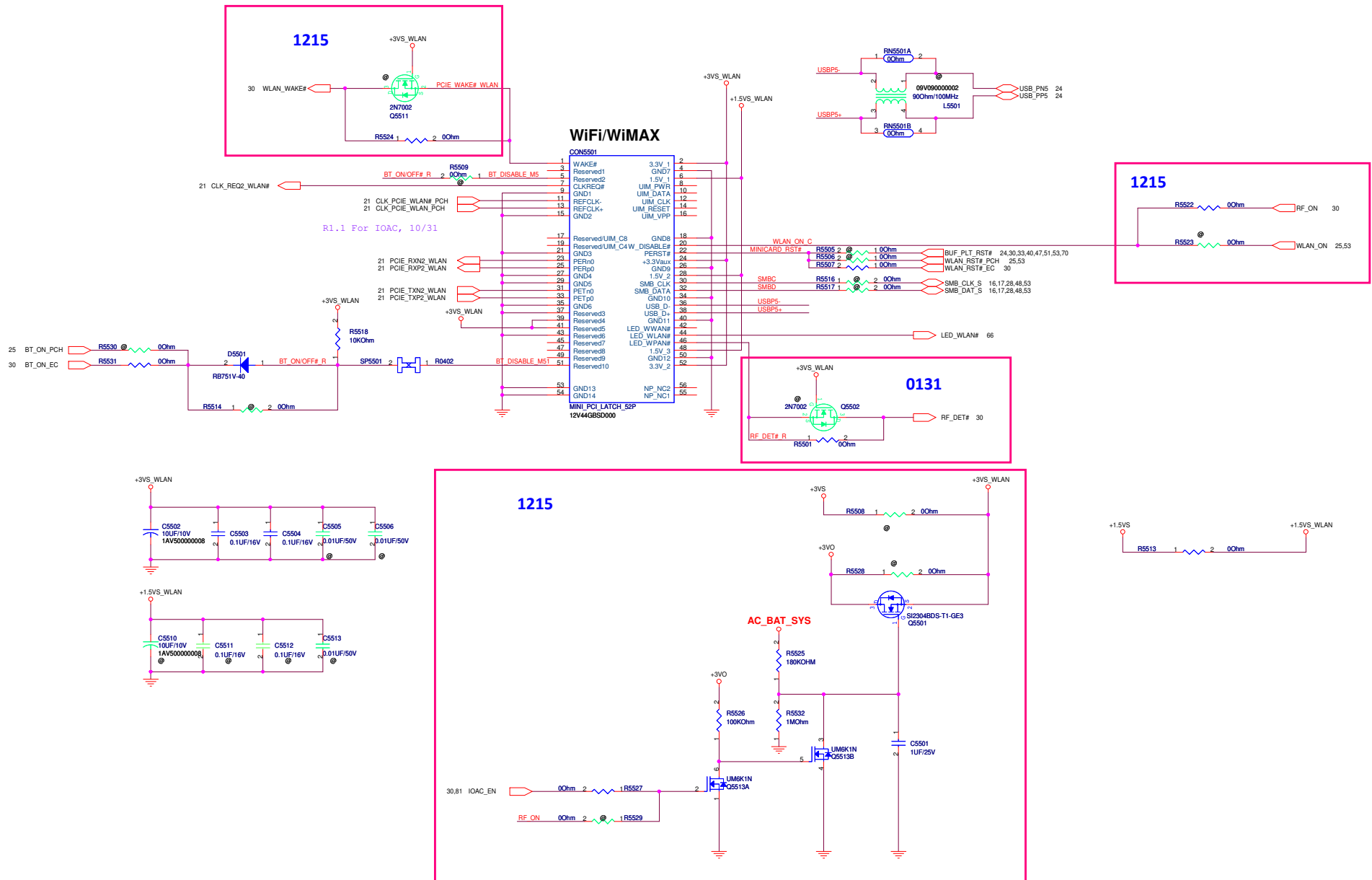
PCIE/mSATA

Select PCIE or mSATA IF select mSATA (only +3VAUX)





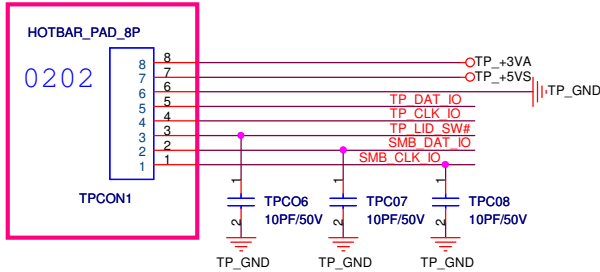
PEGATRON		Title : MINICARD (WUSB /UPCONVERT)	
BU1-RD Div.1+HW RD Dept.1		Engineer: <i>Wing_Cheng</i>	
Size	Project Name		Rev
Custom	BA52HR/CR		1.0
Date: Friday, February 03, 2012		Sheet 54 of 77	



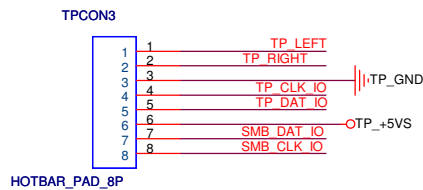
Screw M x 2

Fix Hole J x 1

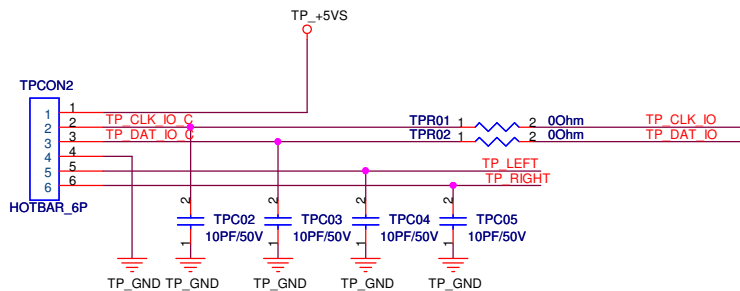
Fix Hole K x 1



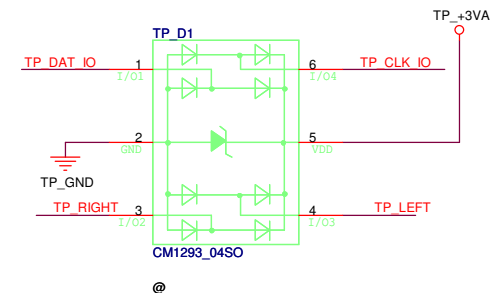
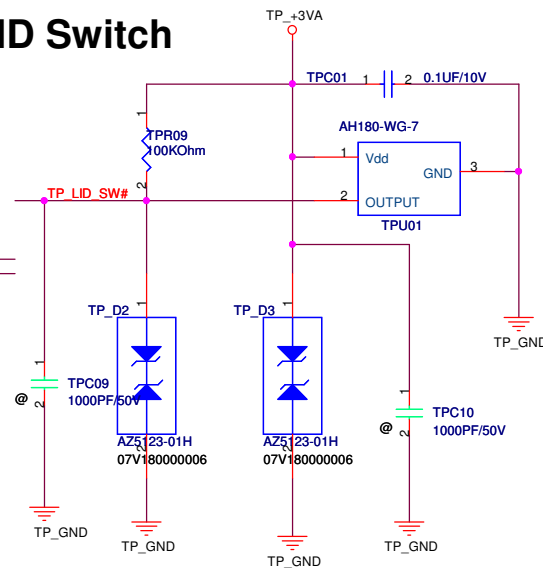
Touch Pad
WIN8



Touch Pad
WIN7



LID Switch

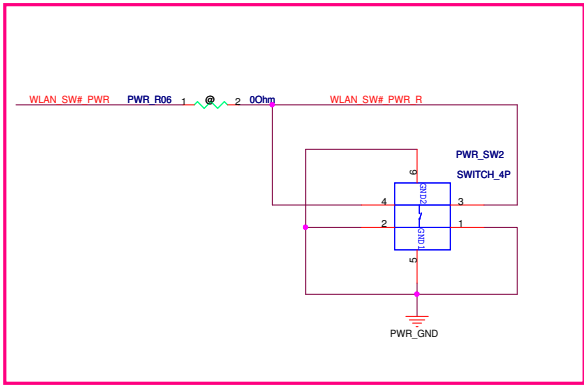
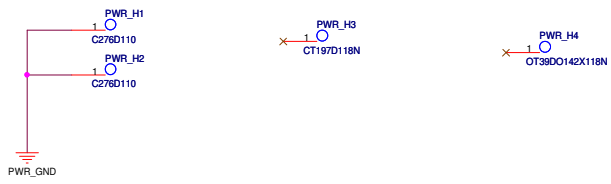


PEGATRON		Title :TP_M	
BG1-HW RD Div.2-NB RD Dept.5		Engineer: Wing_Cheng	
Size B	Project Name BA52HR/CR		Rev 1.0
Date: Friday, February 03, 2012	Sheet	56	of 77

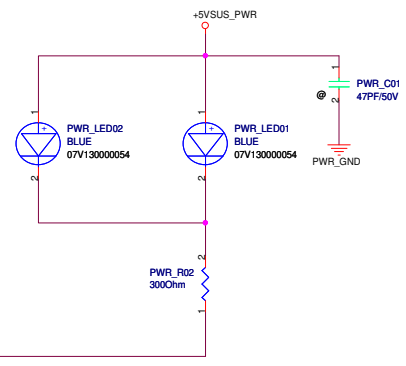
Screw G x 2

Fix Hole H x 1

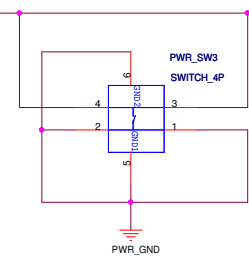
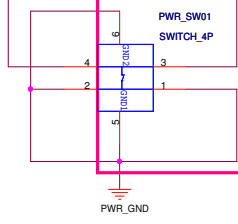
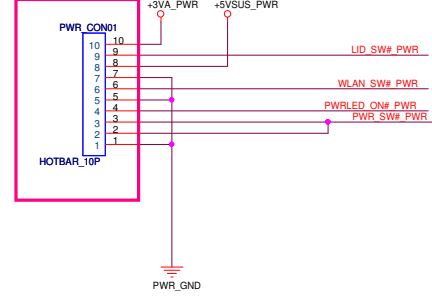
Fix Hole I x 1



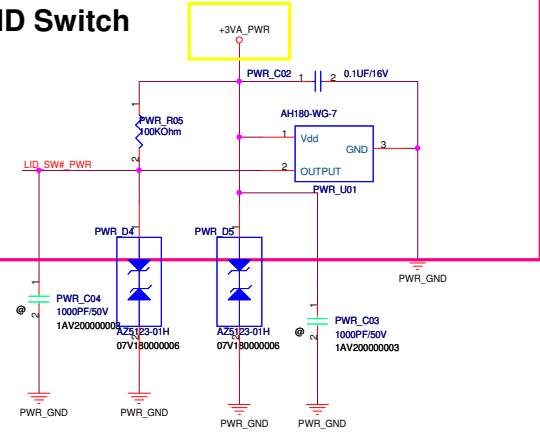
POWER Button LED

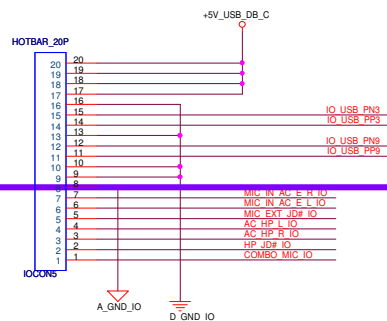


R1.1 reverse PWR_CON01 and change pin 1~4 pin define 1024



LID Switch

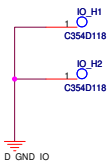




D_GND_IO Moat

A_GND_IO

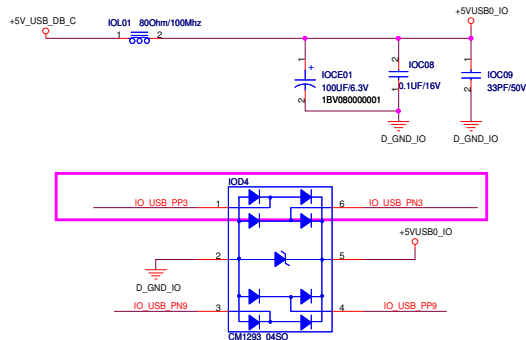
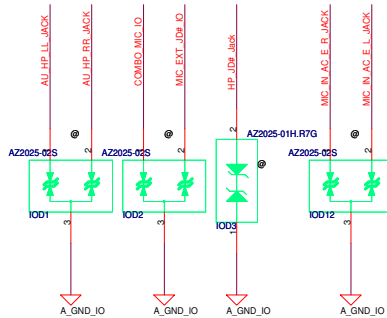
Screw L x 2



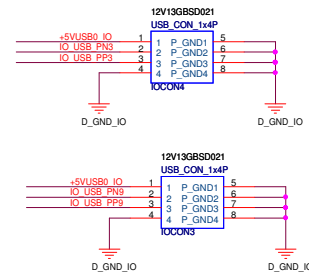
Fix Hole E x 1



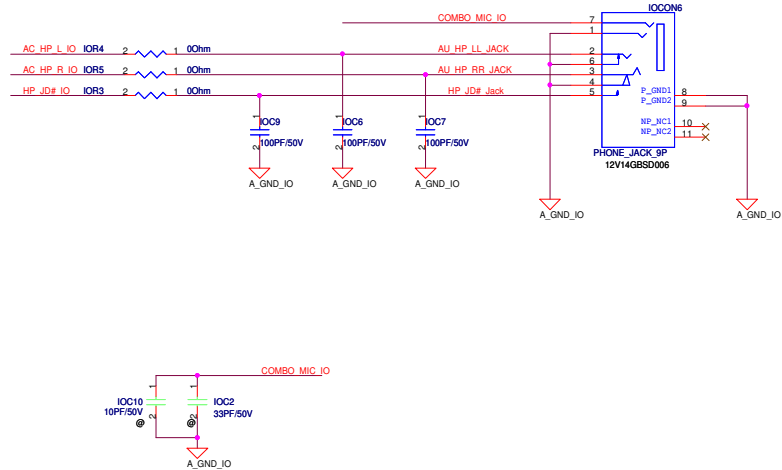
Fix Hole F x 1



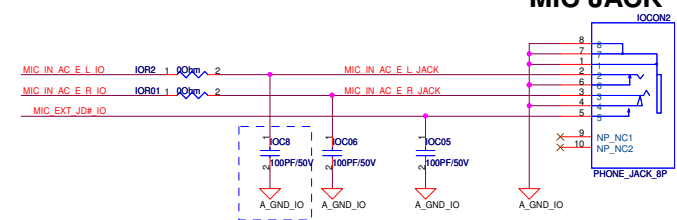
USB 2.0



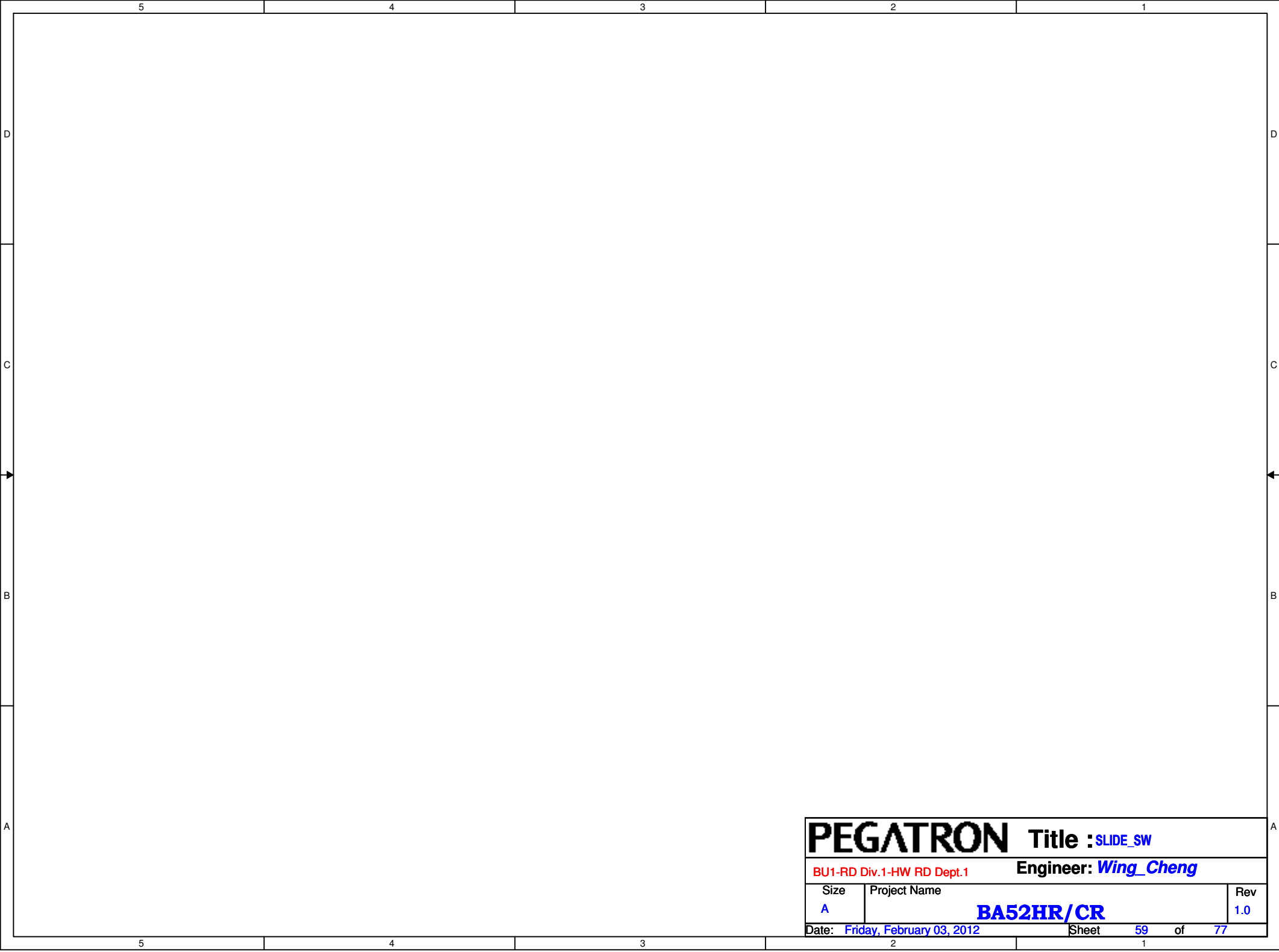
Headphone & MIC combo Jack



MIC JACK



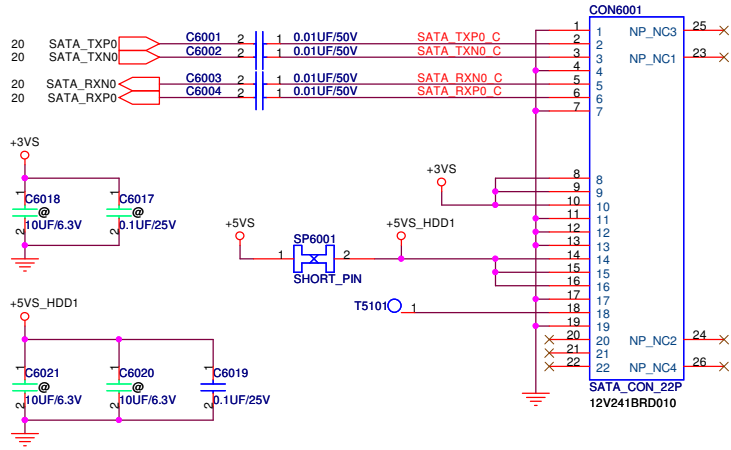
R1.1 Add 2nd MIC schematic 0804



PEGATRON			Title : SLIDE_SW		
BU1-RD Div.1-HW RD Dept.1			Engineer: Wing_Cheng		
Size	Project Name				Rev
A	BA52HR/CR				1.0
Date: Friday, February 03, 2012			Sheet	59	of 77

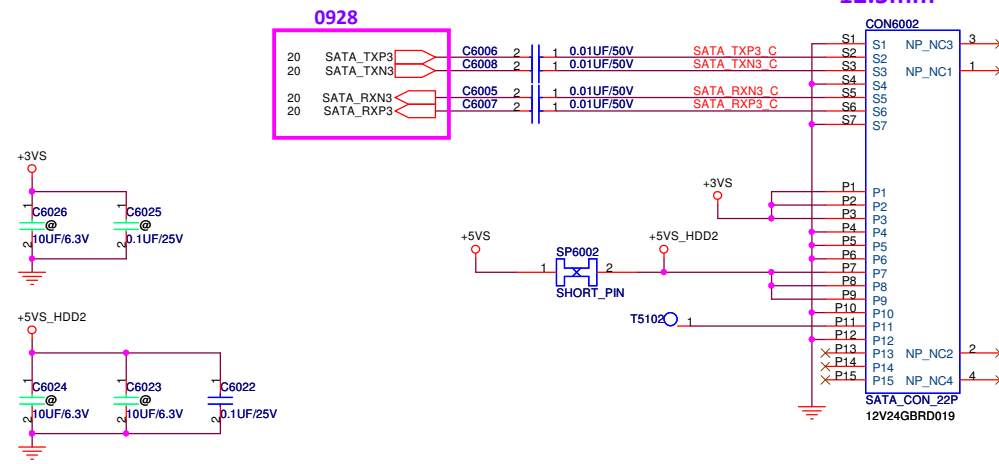
HDD 1

9.5mm



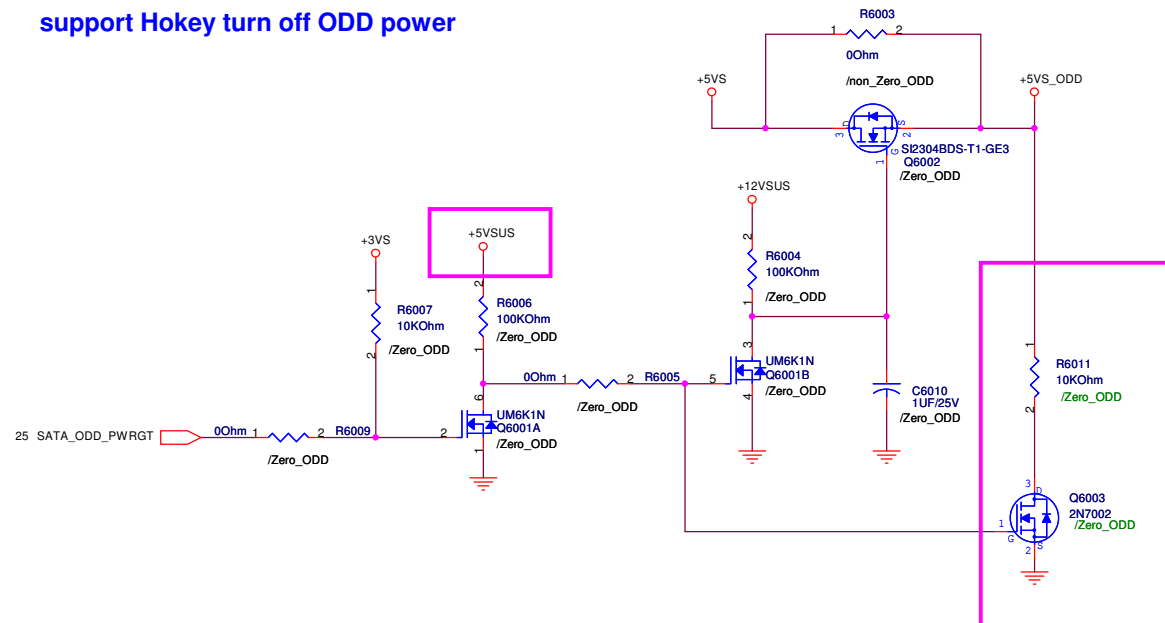
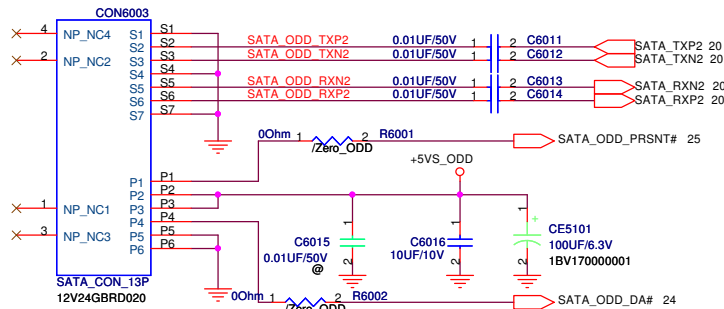
HDD 2

12.5mm

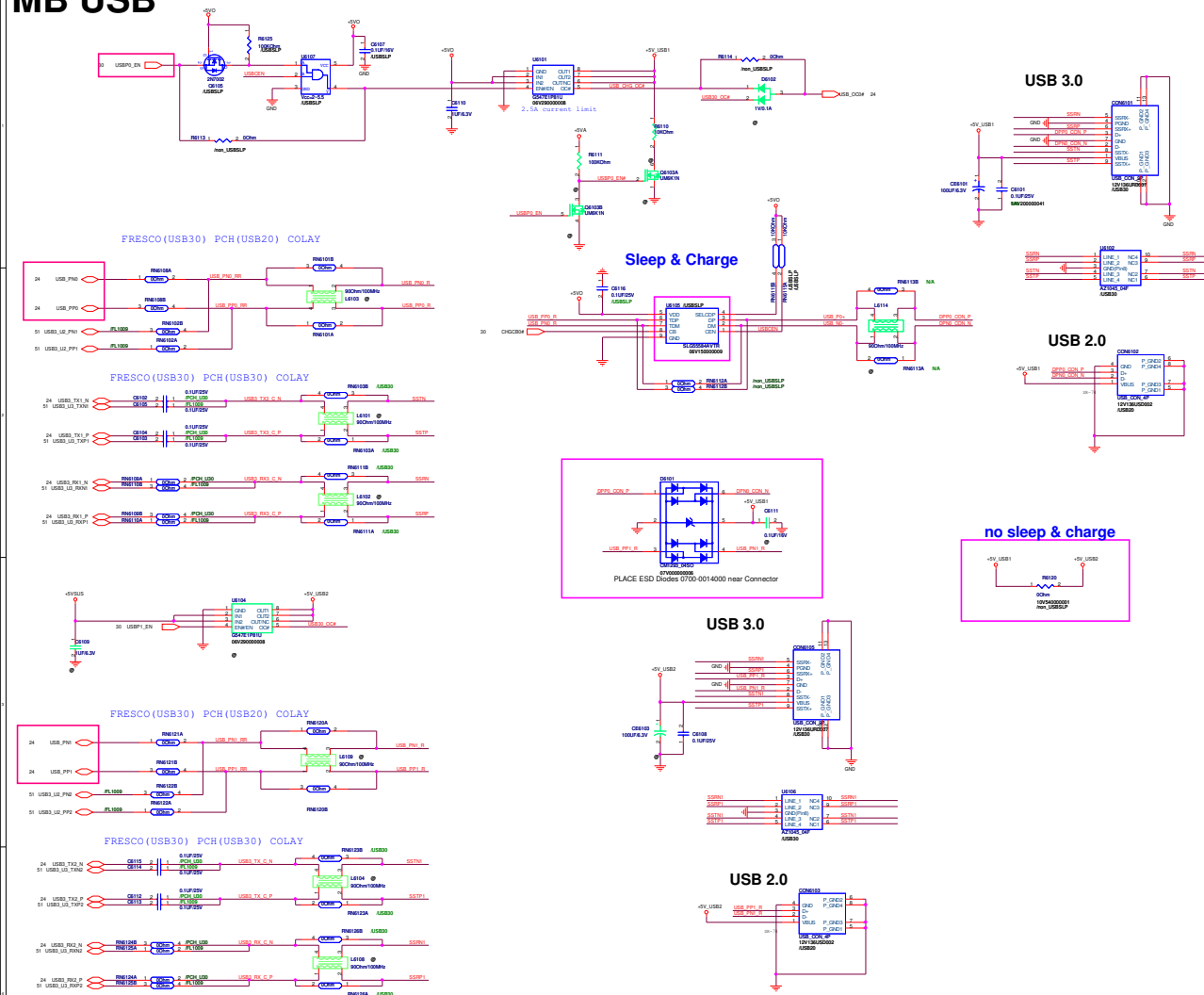


ODD

ZERO POWER ODD SUPPORT support Hokey turn off ODD power



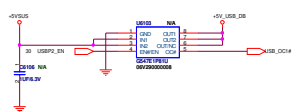
MB USB



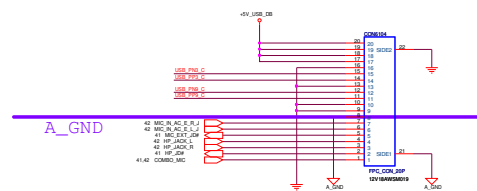
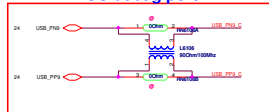
IO Board

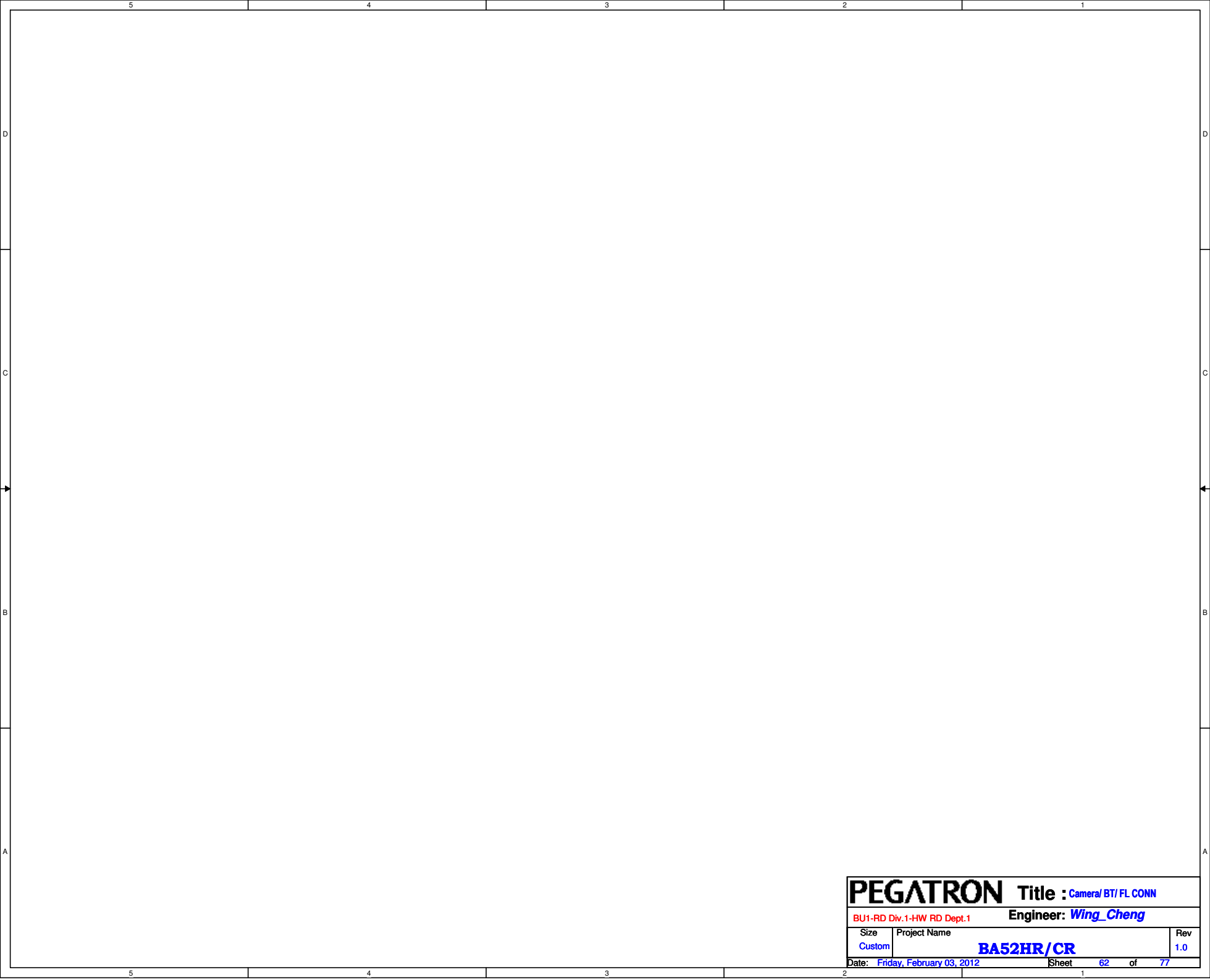
AUDIO BOARD/w USB2.0 x2

USB Power Switch for USB DB Main



BIOS debug port

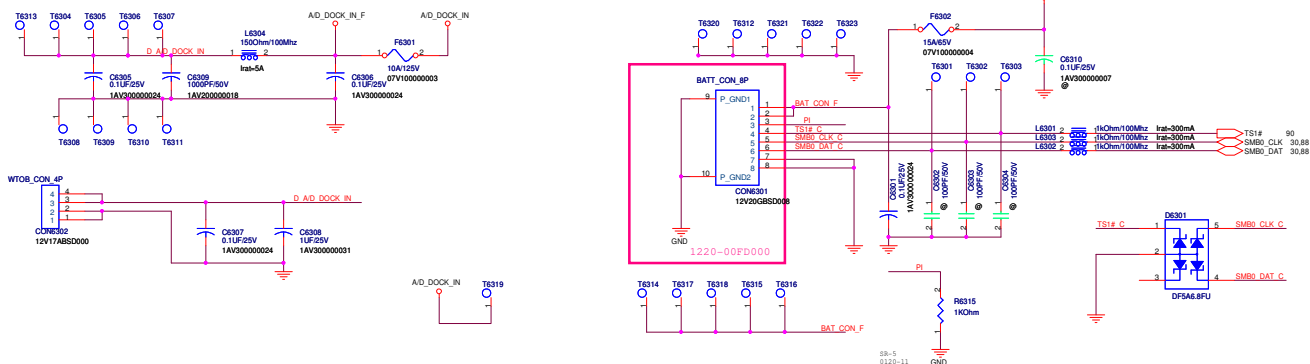




PEGATRON		Title : Camera/ BT/ FL CONN	
BU1-RD Div.1-HW RD Dept.1		Engineer: Wing_Cheng	
Size Custom	Project Name BA52HR/CR		Rev 1.0
Date: Friday, February 03, 2012		Sheet	62 of 77

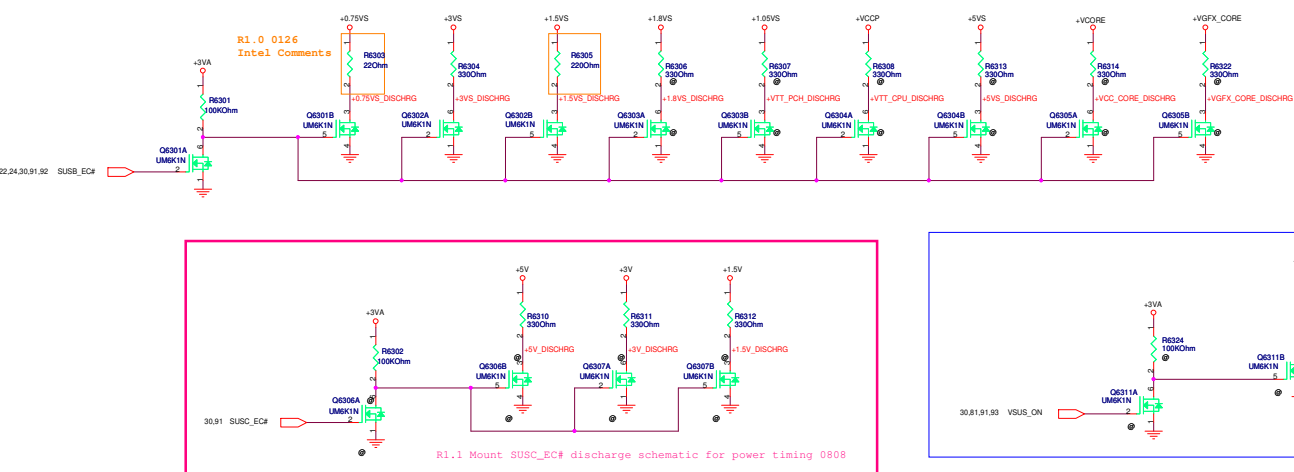
DC IN

Battery Connector

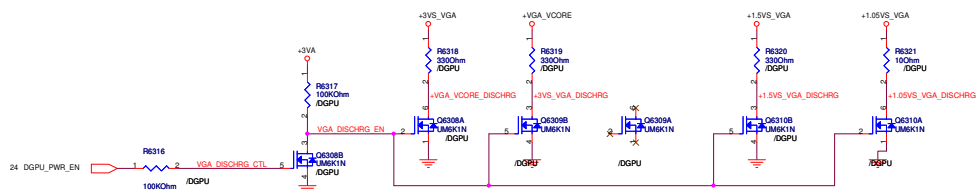


Discharge Circuit

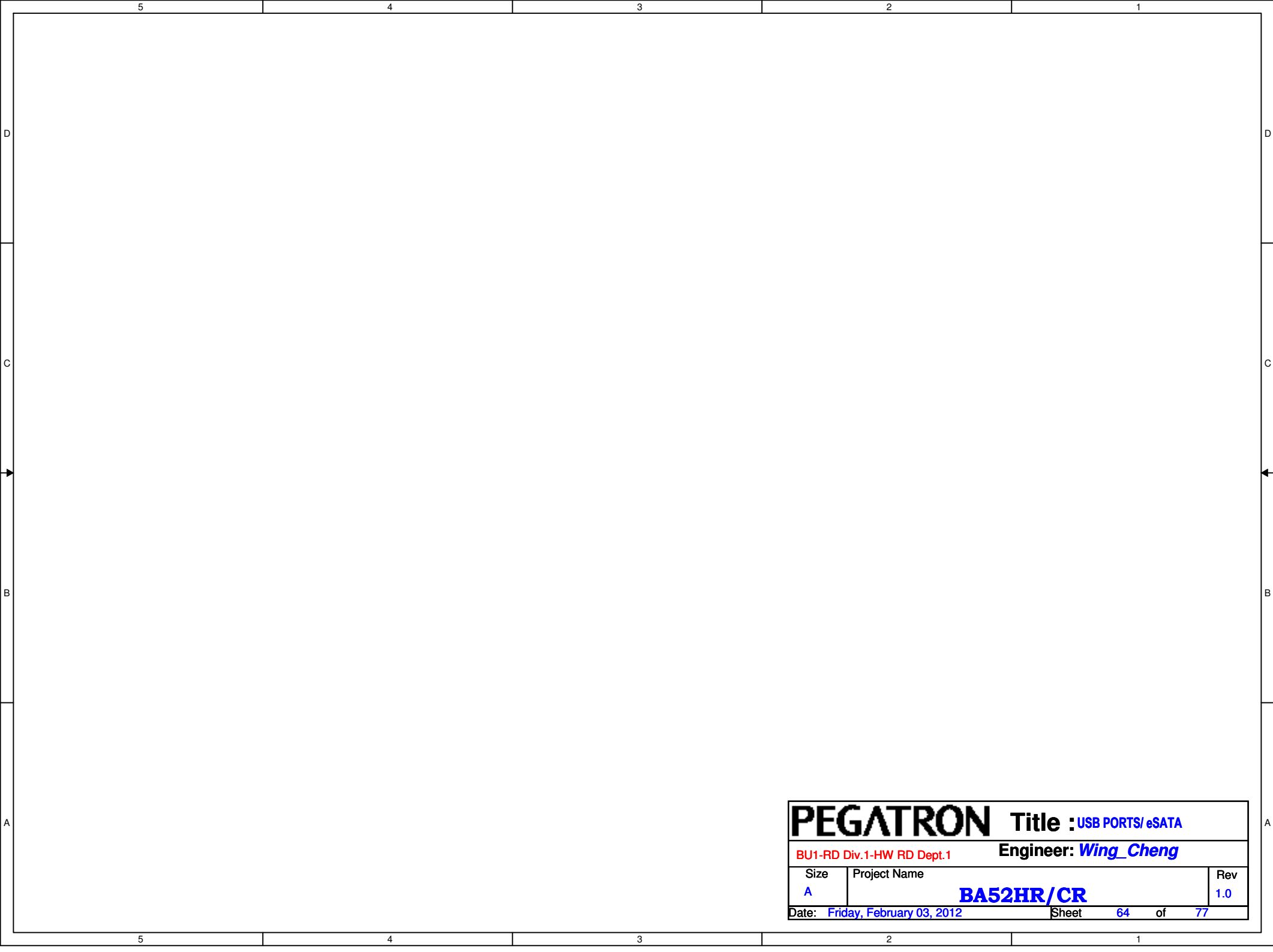
Frank
0505 Follow EVEREST



VGA Discharge Circuit

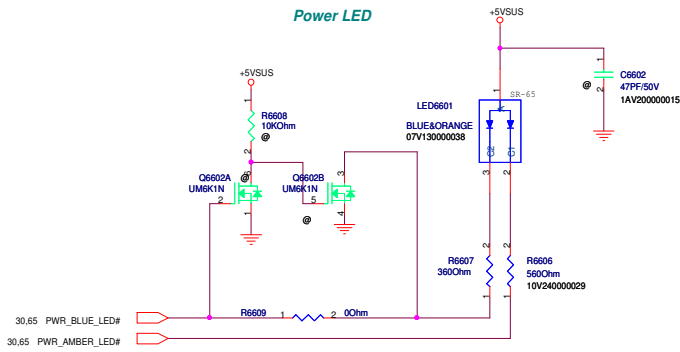


Unmount +VGA_Vcore discharg

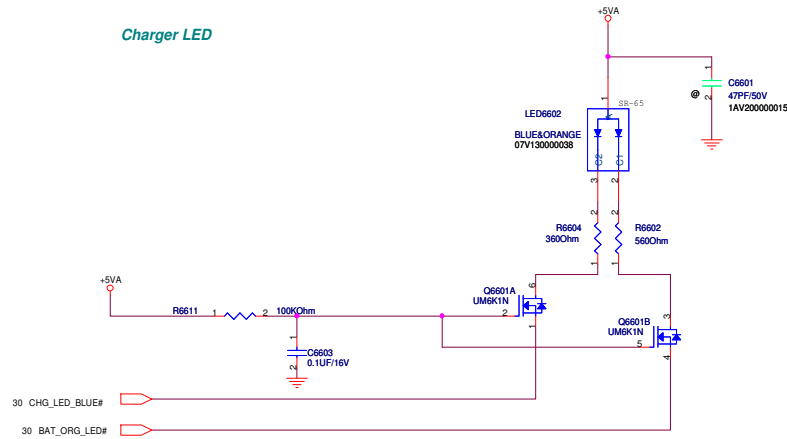


PEGATRON		Title : USB PORTS/ eSATA	
BU1-RD Div.1-HW RD Dept.1		Engineer: Wing_Cheng	
Size A	Project Name BA52HR/CR		Rev 1.0
Date: Friday, February 03, 2012		Sheet	64 of 77

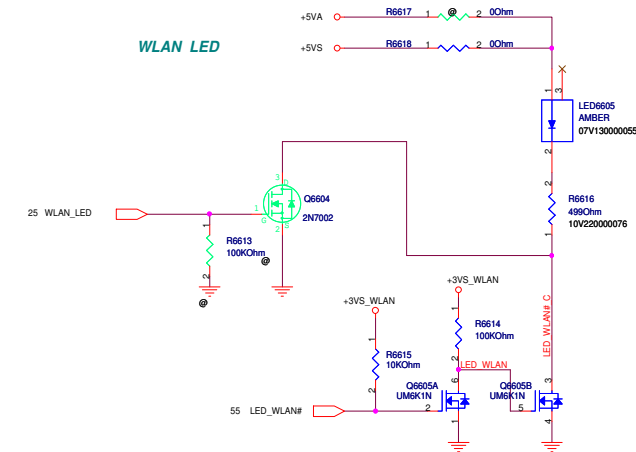
Power LED



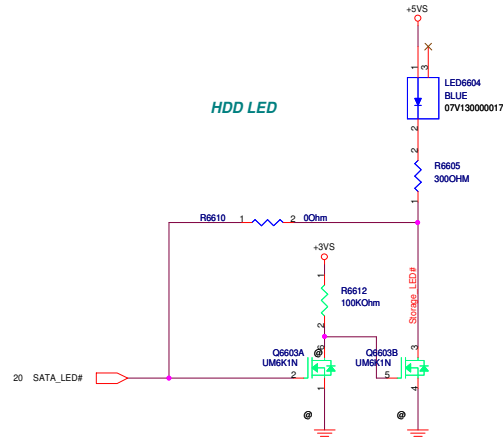
Charger LED



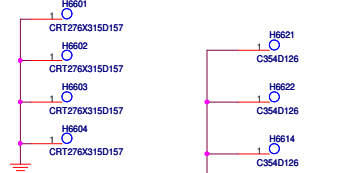
WLAN LED



HDD LED



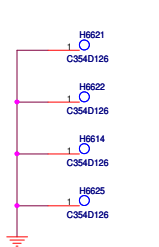
CPU Screw B x 4



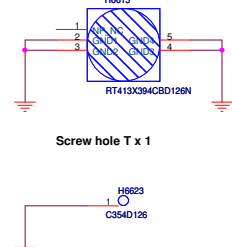
GPU Screw P x 2



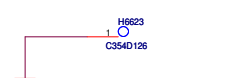
Screw A x 4 (PTH)



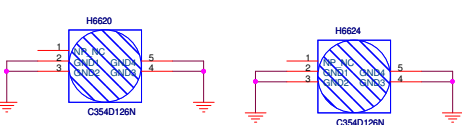
Screw hole R x 1



Screw hole T x 1



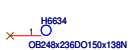
Screw A x 2 (NPTH)



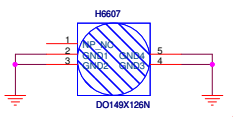
Fix hole D x 1



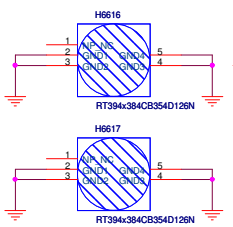
Fix hole N x 1



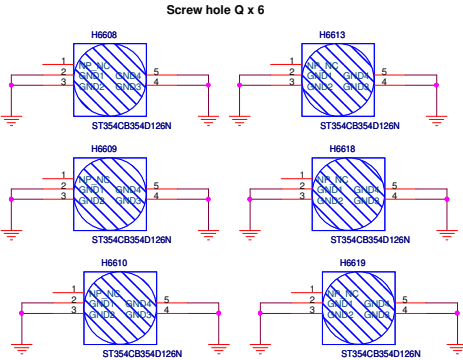
Screw hole V x 1



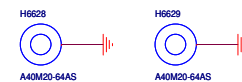
Screw hole S x 2



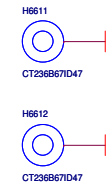
Screw hole Q x 6



WLAN NUT

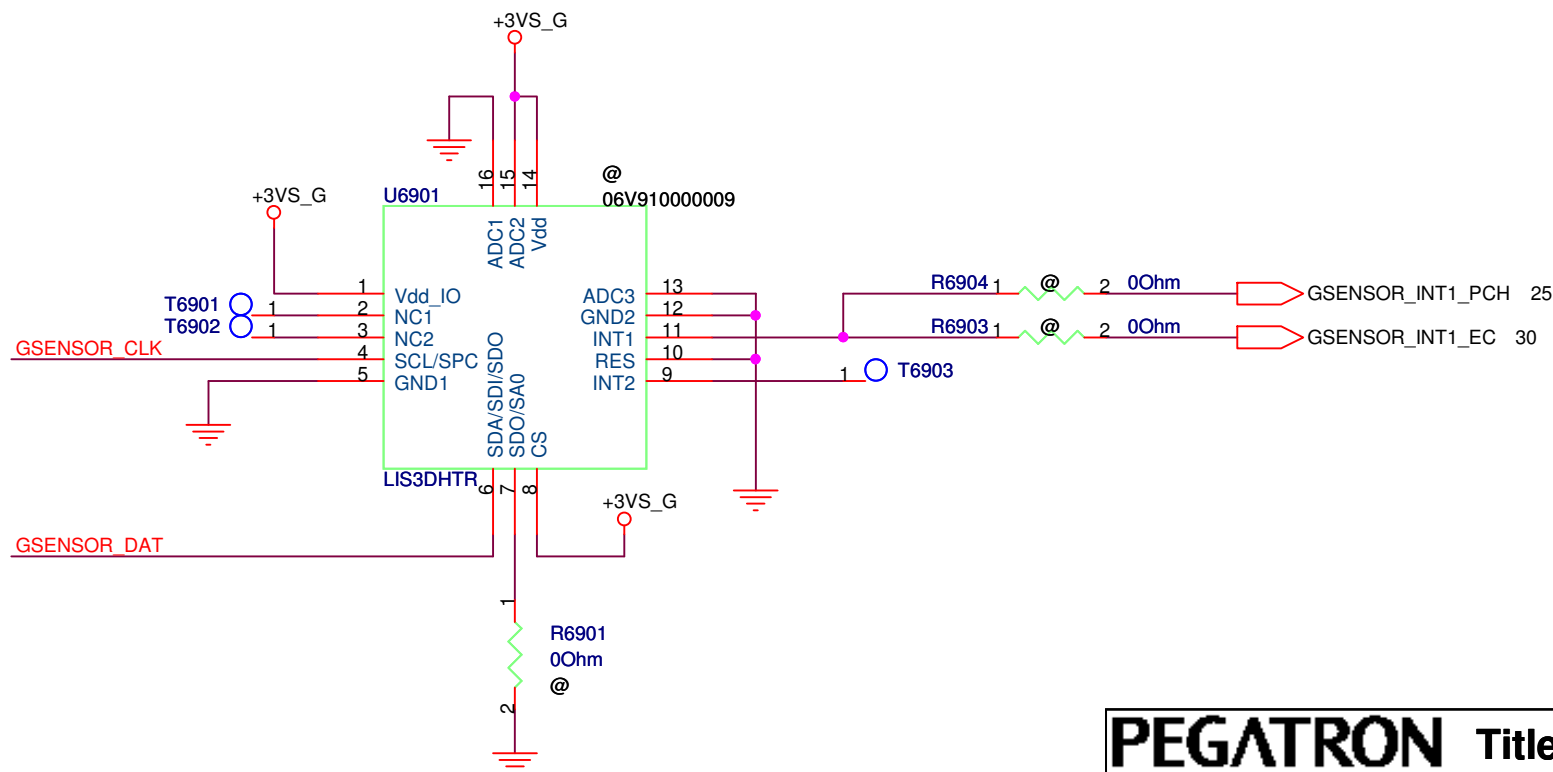
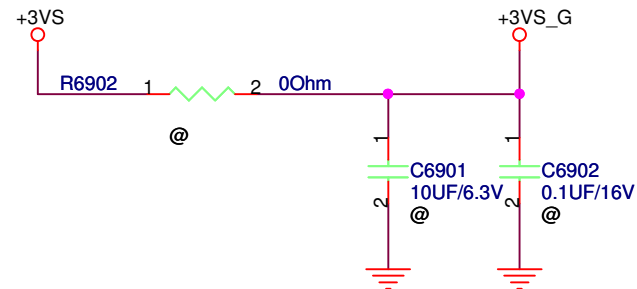
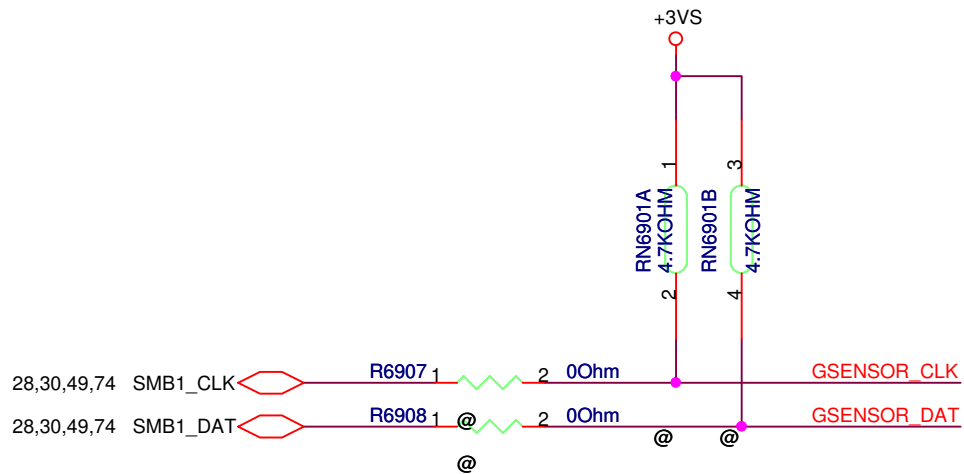


PCH Local Side Symbol



5	4	3	2	1
D				D
C				C
B				B
A				A

PEGATRON		Title : Finger Printer	
Pegatron Corp.		Engineer: Wing_Cheng	
Size A	Project Name BA52HR/CR		Rev 1.0
Date: Friday, February 03, 2012		Sheet	68 of 77



PEGATRON		Title : G-Sensor TSH35TR	
BU1-RD Div.1-HW RD Dept.1		Engineer: Wing_Cheng	
Size A	Project Name		Rev 1.0
Date: Friday, February 03, 2012		Sheet	69 of 77

10/03 Change C7203 optional from /DGPU to @ (Follow NV FAE recommend) (Mickey)
 09/27 Change L7201 from 300ohm bead to 220ohm bead (Follow NV design guide) (Mickey)
 09/27 Change R7202,C7206 optional from /DGPU to /N13P-GS_N13P-GL (Mickey)
 09/26 Change R7201 optional from /DGPU to /OPT (Mickey)
 09/26 Change C7201~7205,L7201 optional from /DGPU to /DGPU (Mickey)

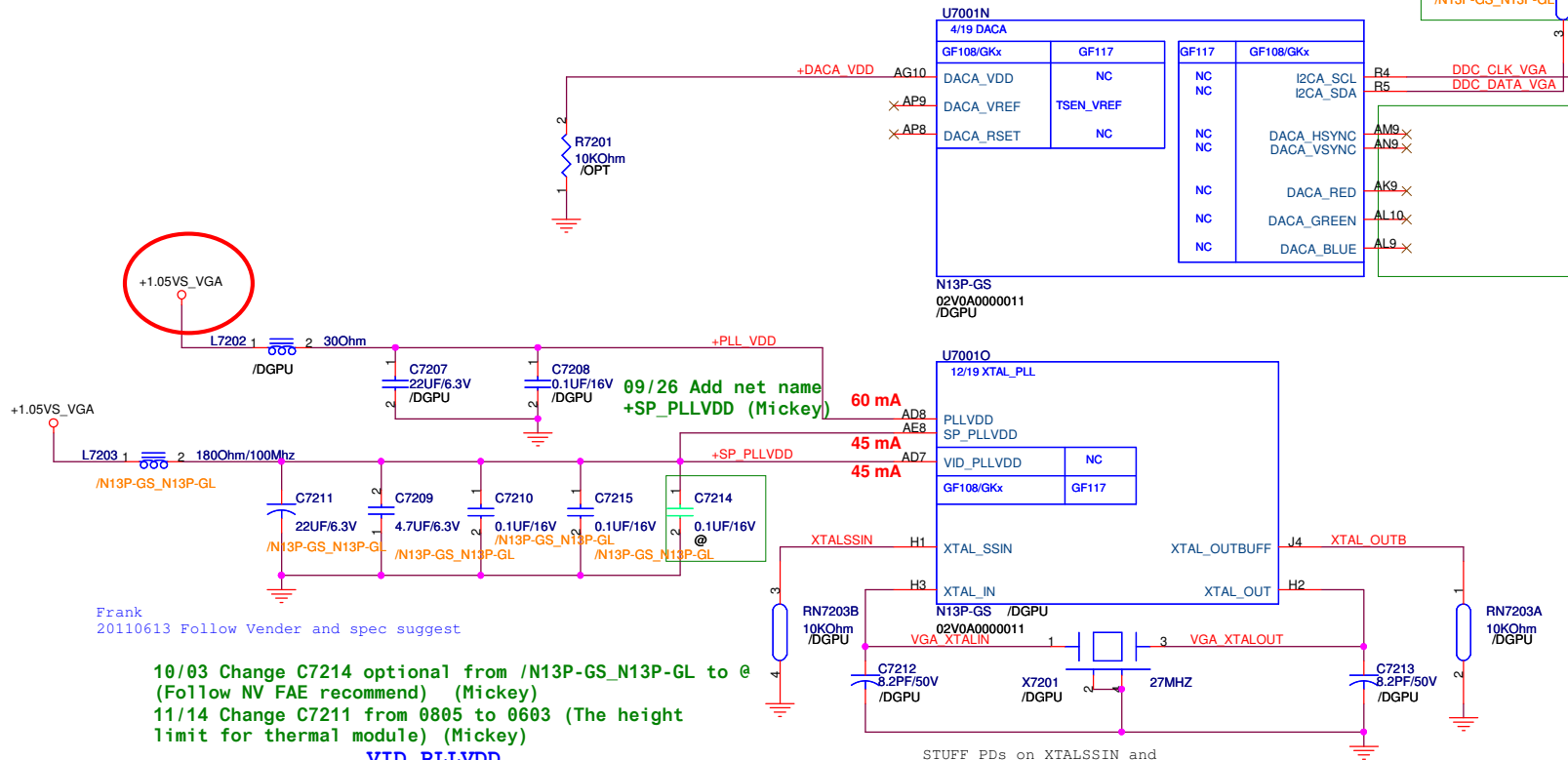
RGB	
N13M-GS	N13P-GL/N13P-GS
NC	RGB Function

RN7201B 2.2KOhm /N13P-GS_N13P-GL	RN7201A 2.2KOhm /N13P-GS_N13P-GL
--	--

09/26 Change RN7201 optional from /DGPU to /N13P-GS_N13P-GL (Mickey)

09/29 Correct the net name of DDC_CLK_VGA, DDC_DATA_VGA, DAC_HSYNC_VGA and DAC_VSYNC_VGA (Mickey)

11/29 Remove net DAC_HSYNC_VGA, DAC_VSYNC_VGA, DAC_VR, DAC_VG, DAC_VB for VGA_Vcore power plane improvement(EImer)



Frank
 20110613 Follow Vender and spec suggest

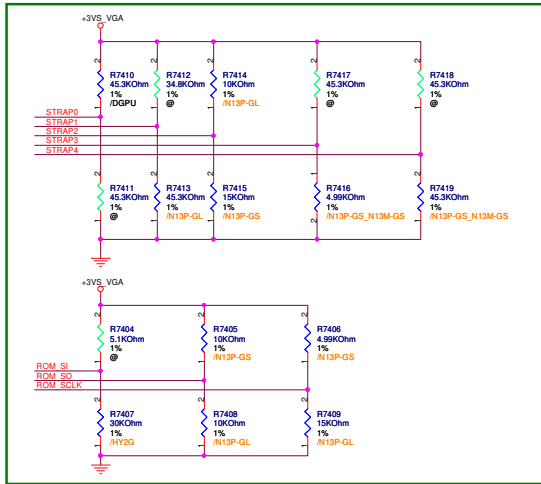
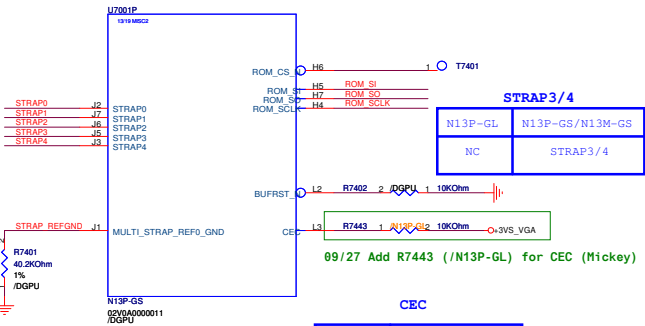
10/03 Change C7214 optional from /N13P-GS_N13P-GL to @ (Follow NV FAE recommend) (Mickey)
 11/14 Change C7211 from 0805 to 0603 (The height limit for thermal module) (Mickey)

VID_PLLVDD

N13M-GS	N13P-GL/N13P-GS
NC	VID_PLLVDD (1.05V)

11/16 Change C7212,C7213 from 18pF to 8.2pF (Crystal vendor recommend) (Mickey)

PEGATRON		Title : GPU_RGB/XTAL	
PEGATRON COMPUTER INC		Engineer: Mickey_Yu	
Size B	Project Name P/N	VA70_N13P-GDDR3	Rev 1.0
Date: Friday, February 03, 2012		Sheet 72 of 99	



N13P-GS ES2/QS			
DEVICE ID	0xFDB		
STRAP0	45K PU		
STRAP1	35K PD		
STRAP2	15K PD		
STRAP3	5K PD		
STRAP4	10K PD		
ROM_SCLK	5K PU		
ROM_SI	Hynix 128Mx16	35K PD	R7407
ROM_S0	Hynix 64Mx16	15K PD	

STRAP2--GPU TYPE		
N13M-GS	N13P-GL	N13P-GS

ROM_SI--VRAM TYPE			
HYNIX		SAMSUNG	
64Mx16	128Mx16	64Mx16	128Mx16

N13P-GS GL QS			
DEVICE ID	0xDE9		
STRAP0	45K PU		
STRAP1	45K PD		
STRAP2	10K PU		
STRAP3	NC		
STRAP4	NC		
ROM_SCLK	15K PD		
ROM_SI	Hynix 128Mx16	35K PD	
ROM_S0	Hynix 64Mx16	15K PD	R7407

STRAP1	N13P-GS ES2/QS	N13P-GL QS
R7413	35K	45K

ROM_SI	Hynix 128Mx16	Hynix 64Mx16
R7407	35K	15K

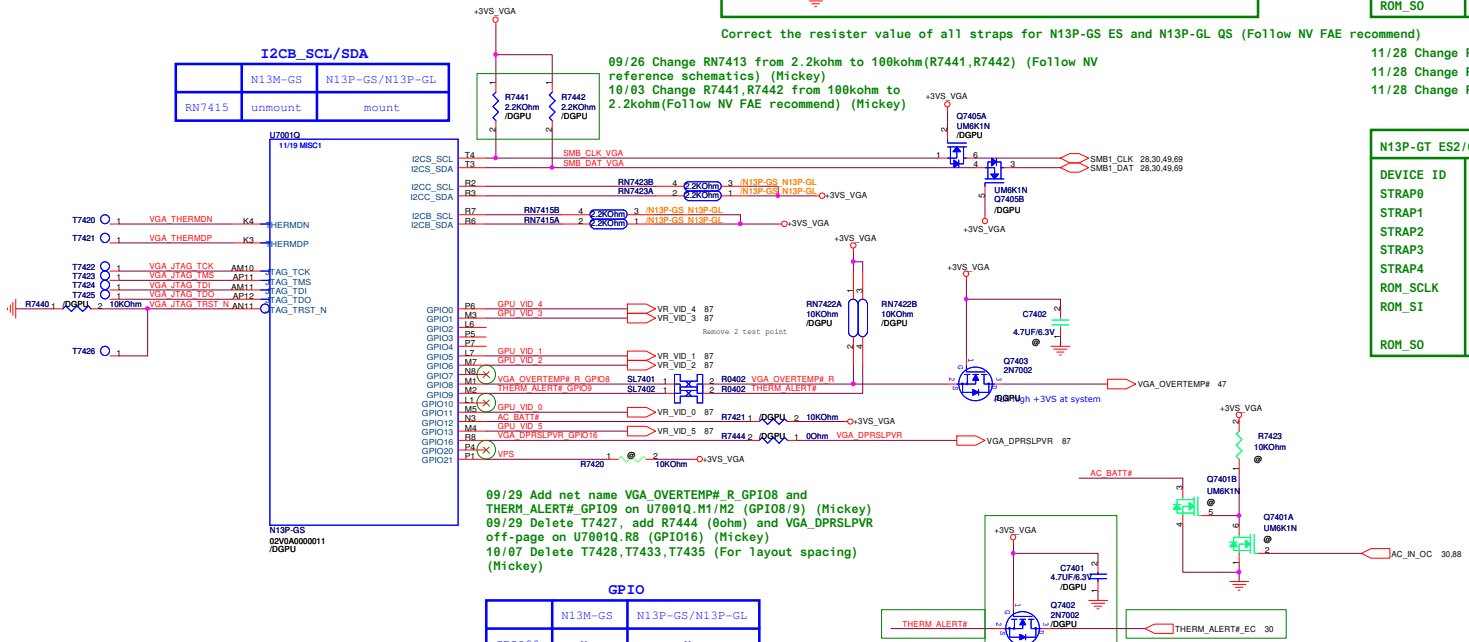
Correct the resistor value of all straps for N13P-GS ES and N13P-GS GL QS (Follow NV FAE recommend)

- 11/28 Change R7413 from /DGPU to /N13P-GS (Follow NV FAE recommend) (Mickey)
- 11/28 Change R7414 from 20kohm to 10kohm(/N13P-GL) (Follow NV FAE recommend) (Mickey)
- 11/28 Change R7415 from 5kohm to 15kohm(/N13P-GS) (Follow NV FAE recommend) (Mickey)

I2CB_SCL/SDA		
N13M-GS	N13P-GS/N13P-GL	
RN7415	unmount	mount

- 09/26 Change RN7413 from 2.2kohm to 100kohm(R7441,R7442) (Follow NV reference schematics) (Mickey)
- 10/03 Change R7441,R7442 from 100kohm to 2.2kohm(Follow NV FAE recommend) (Mickey)

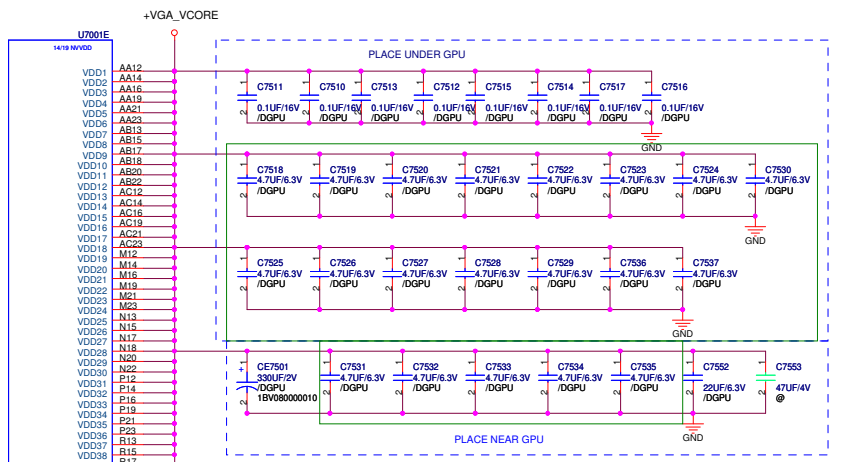
N13P-GT ES2/QS			
DEVICE ID	0xFD1		
STRAP0	45K PU		
STRAP1	35K PD		
STRAP2	10K PD		
STRAP3	5K PD		
STRAP4	10K PD		
ROM_SCLK	5K PU		
ROM_SI	Hynix 128Mx16	35K PD	
ROM_S0	Hynix 64Mx16	15K PD	R7407



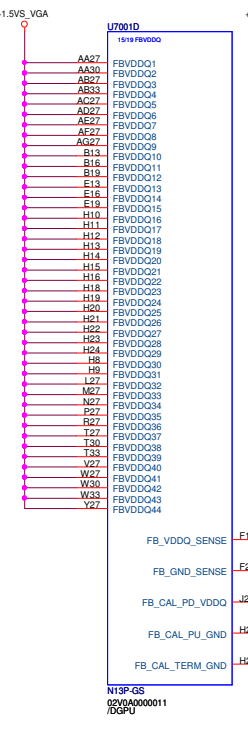
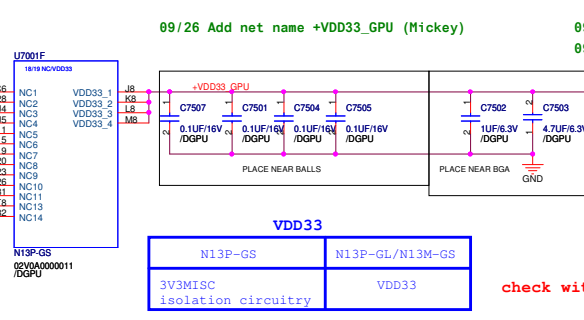
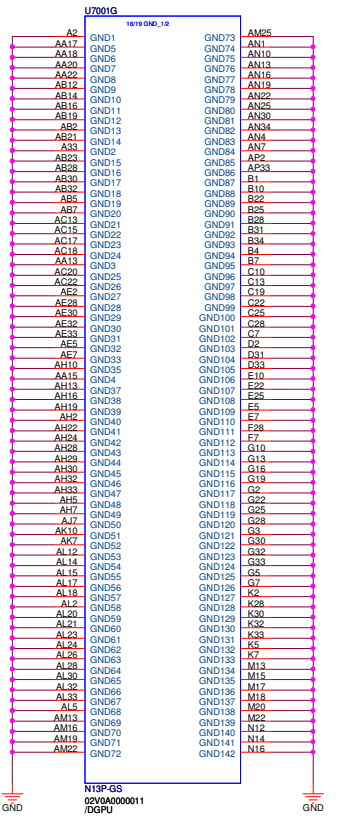
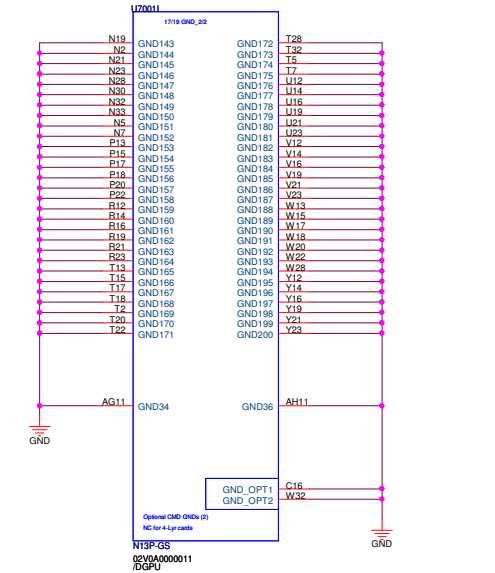
- 09/29 Add net name VGA_OVERTEMP#_R GPIO8 and THERM_ALERT# GPIO9 on U7001Q.M1/M2 (GPIO8/9) (Mickey)
- 09/29 Delete T7427, add R7444 (0ohm) and VGA DPRSLPVR off-page on U7001Q.R8 (GPIO16) (Mickey)
- 10/07 Delete T7428,T7433,T7435 (For layout spacing) (Mickey)

GPIO		
	N13M-GS	N13P-GS/N13P-GL
GPIO20	X	X
GPIO21	X	X

GPIO 8		
	N13P-GL	N13P-GS/N13M-GS
Q7403	unmount	NV suggestion mount

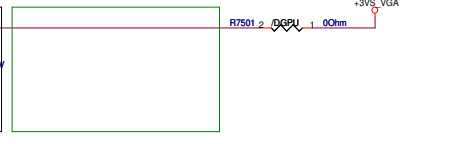


09/29 Change C7518-C7537 from 10uF to 4.7uF (Follow NV design guide) (Mickey)



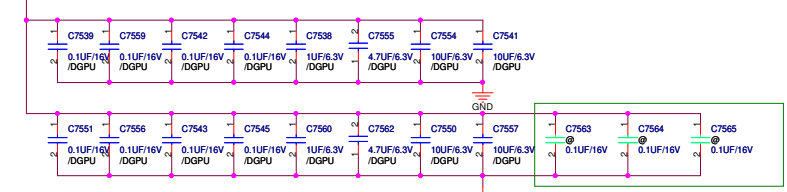
VDD33	
N13P-GS	N13P-GL/N13M-GS
3V3MISC	VDD33
isolation circuitry	

09/26 Add net name +VDD33_GPU (Mickey)
09/26 Add C7506,C7508,C7509 (Follow NV reference schematics) (Mickey)
09/27 Remove C7506,C7508,C7509 (Follow NV design guide) (Mickey)



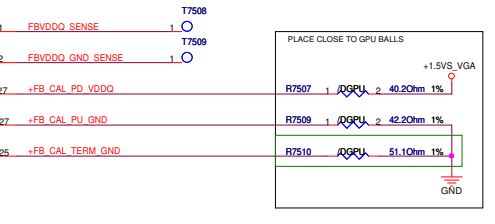
check with NV==>可先不用Isolation circuitry

Frank
20110613 Follow Vender and spec suggest
=> Add C7542, C7543, C7544, C7545 and C7556 mount
Remove C7540, C7561, C7558, C7649
Change C7541, C7557 to 10uF



11/21 Add C7563,C7564,C7565 (0.1uF) at +1.5VS_VGA (EMI Recommend) (Mickey)

CALIBRATION PIN	QDQPS
FB_CALA_PD_VDDQ	40
FB_CALA_PLU_GND	40
FB_CALA_TERM_GND	60



09/28 Change R7510 from 60.4ohm to 51.1ohm (Follow NV design guide) (Mickey)

Frank
20110613 Follow Vender and spec suggest=>Remove R7509 change 42.2 ohm

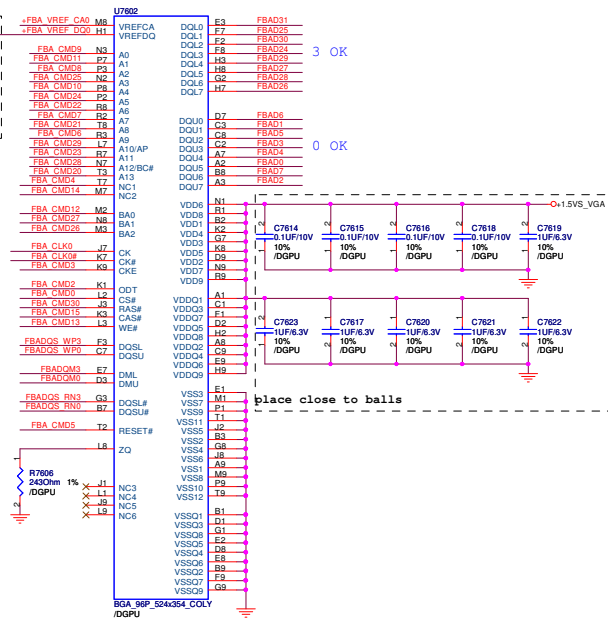
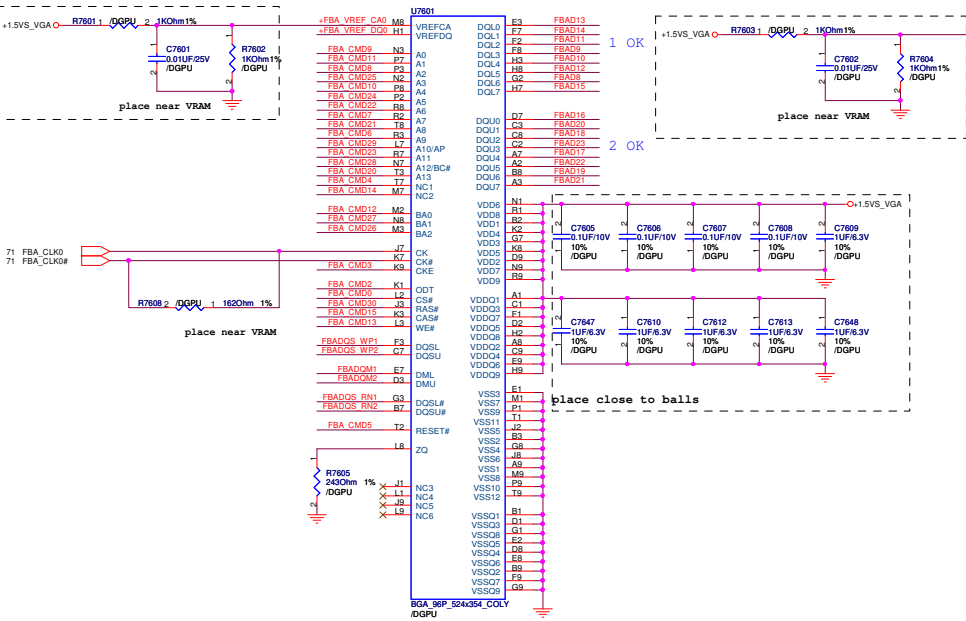
VRAM CH A

TOP SIDE

BOT SIDE

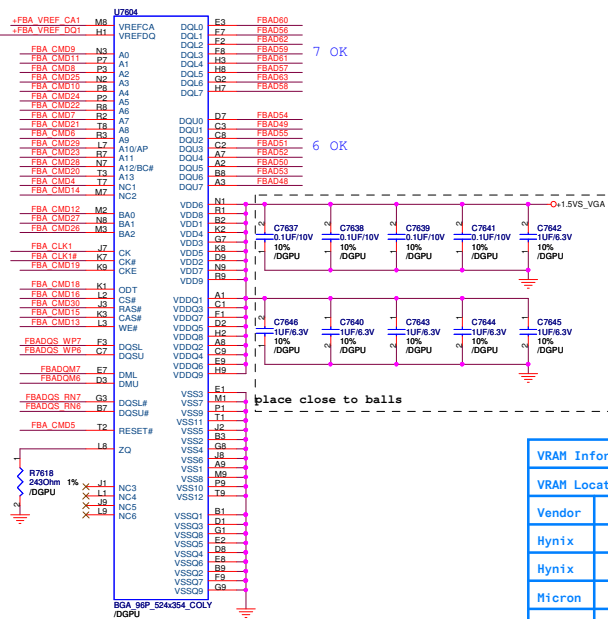
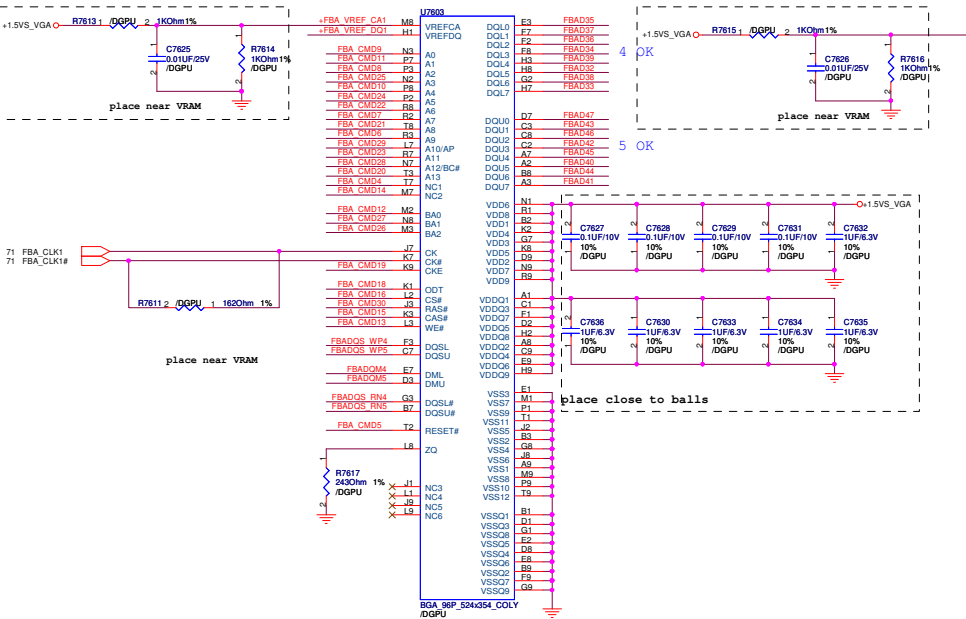
09/27 Swap VRAM data signal. (Mickey)

M13X DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
CMD0	CS0#	
CMD1		
CMD2	ODT	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE#	WE#
CMD14	A15	A15
CMD15	CAS#	CAS#
CMD16	CS0#	
CMD17		
CMD18		ODT
CMD19		CKE
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS#	RAS#
CMD31		



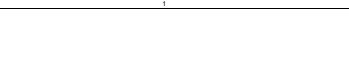
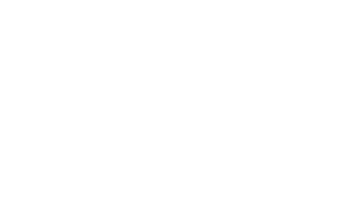
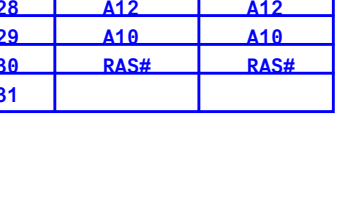
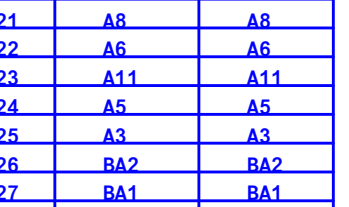
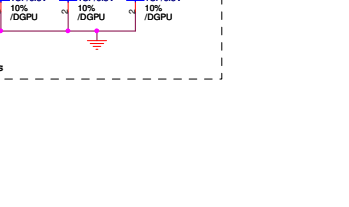
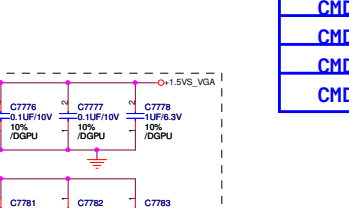
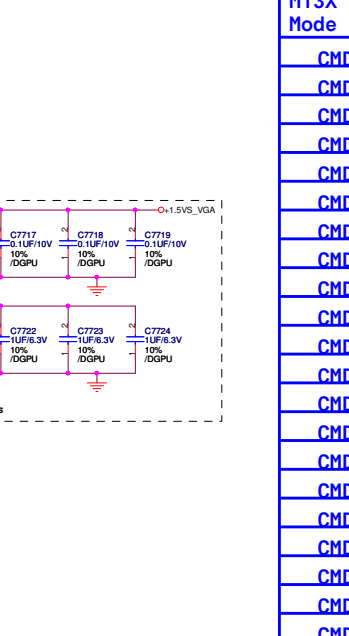
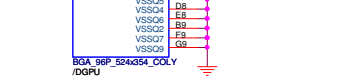
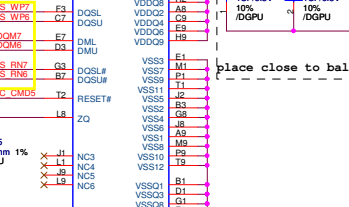
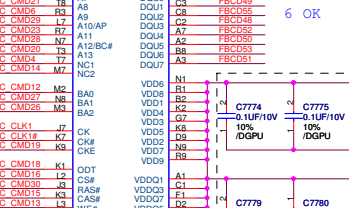
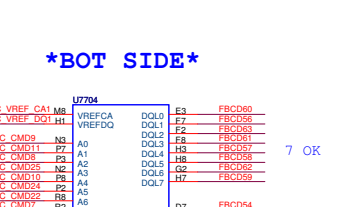
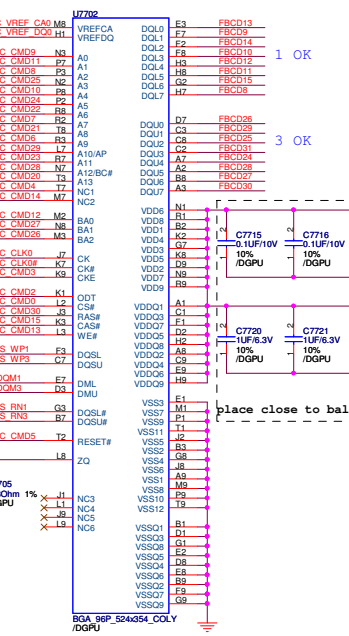
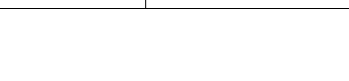
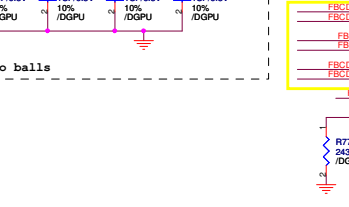
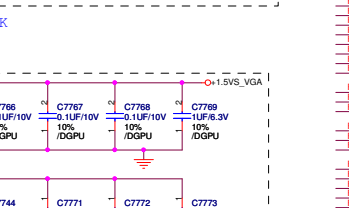
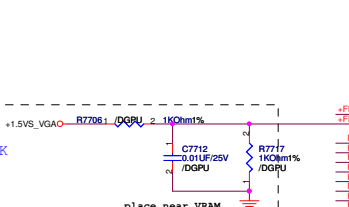
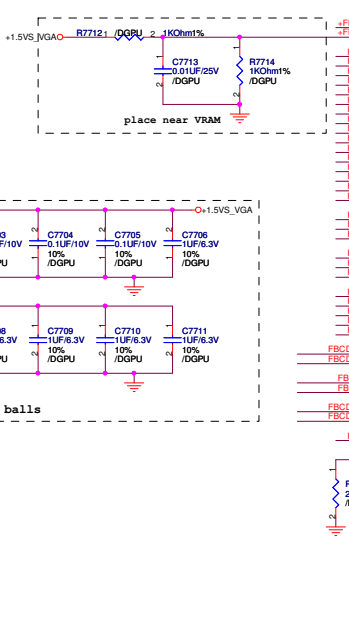
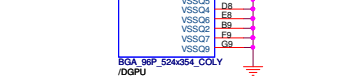
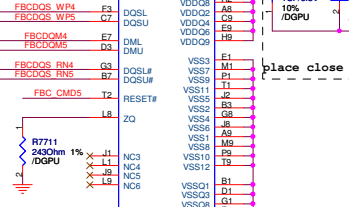
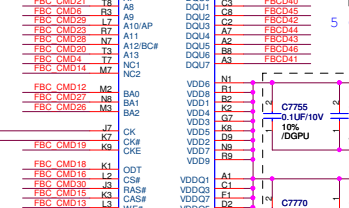
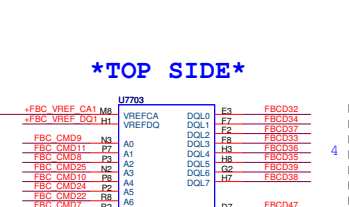
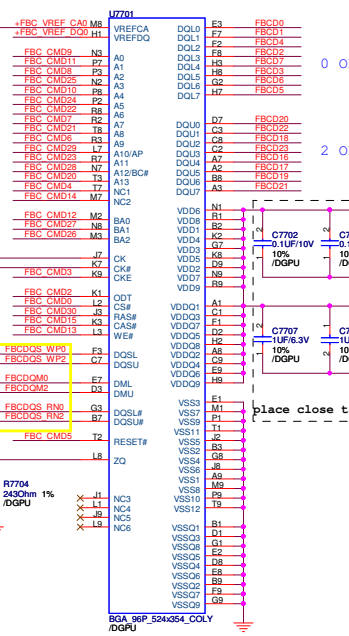
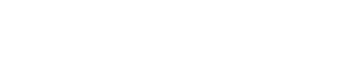
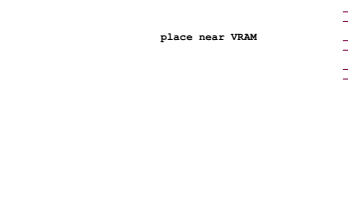
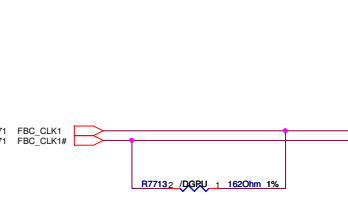
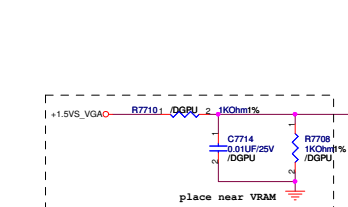
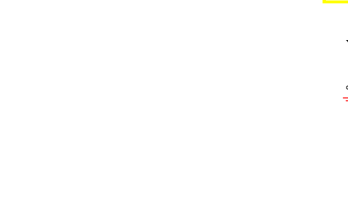
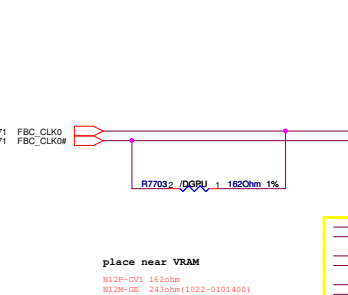
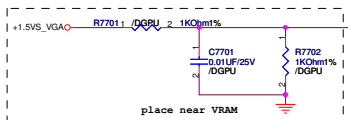
TOP SIDE

BOT SIDE



VRAM Information				VRAM Strap	
VRAM Location : U7601,U7602,U7603,U7604,U7701,U7702,U7703,U7704				VRAM Strap Location : R7487	
Vendor	Configuration	Pegatron P/N	Manufacturer P/N		
Hynix	128Mx16	0315-00ND0PB	H5TQ2663BFR-11C	0x6	35K
Hynix	64Mx16	0315-00NF0PB	H5TQ1G63DFR-11C	0x2	15K
Micron	128Mx16	TBD	MT41J128M16JT-107G:K	TBD	TBD
Micron	64Mx16	0315-00SG0PB	MT41J64M16JT-107G:G	TBD	TBD

VRAM CH C



BOT SIDE

99/27 Swap VRAM data signal. (Mickey)

M13X DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
CMD0	CS0#	
CMD1		
CMD2	ODT	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE#	WE#
CMD14	A15	A15
CMD15	CAS#	CAS#
CMD16		CS0#
CMD17		
CMD18		ODT
CMD19		CKE
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS#	RAS#
CMD31		

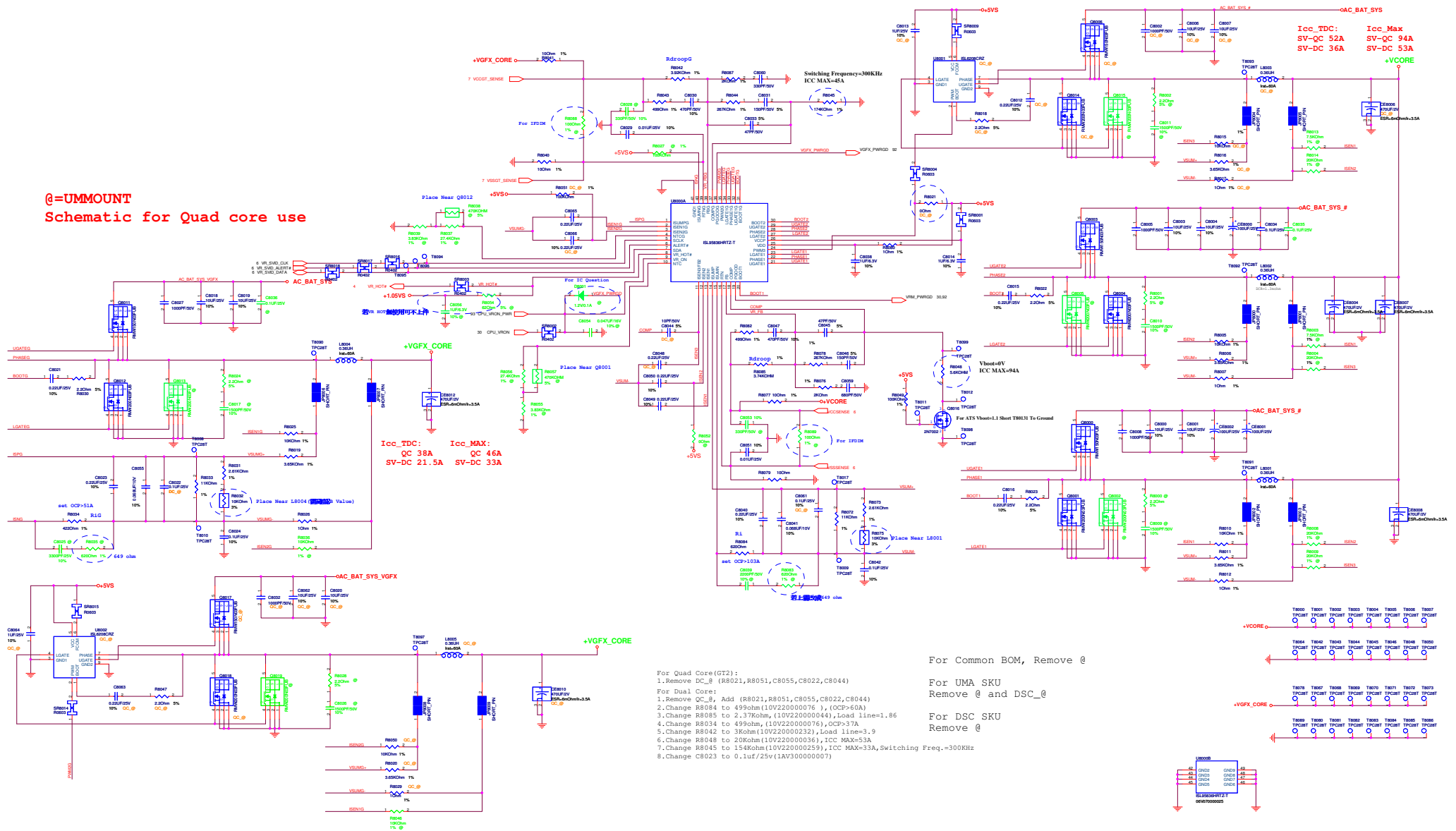
5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

PEGATRON		Title :	
PEGATRON COMPUTER INC		Engineer: Mickey_Yu	
Size	Project Name		Rev
C	P/N	VA79_N13P-GDDR3	1.0
Date: Friday, February 03, 2012		Sheet	79 of 99

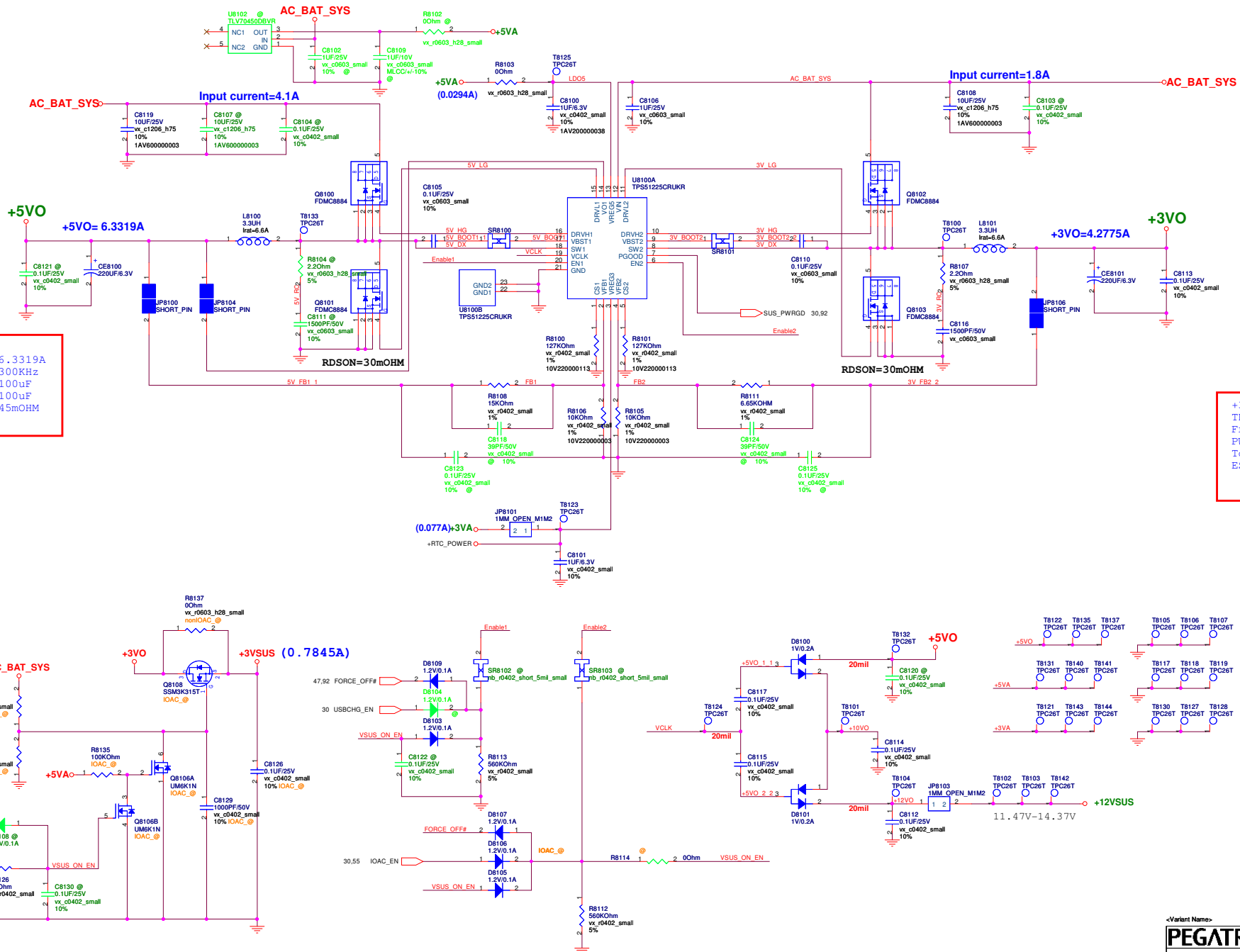


PEGATRON		Title : GPU_PEG*16	
PEGATRON COMPUTER INC		Engineer: Mickey_Yu	
Size	Project Name	Rev	
C	P/N	1.0	
Date: Friday, February 03, 2012		Sheet	79 of 99

@=UMMOUNT
Schematic for Quad core use

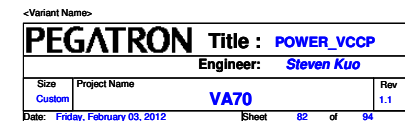


+5V0 & +3V0 POWER SUPPLY

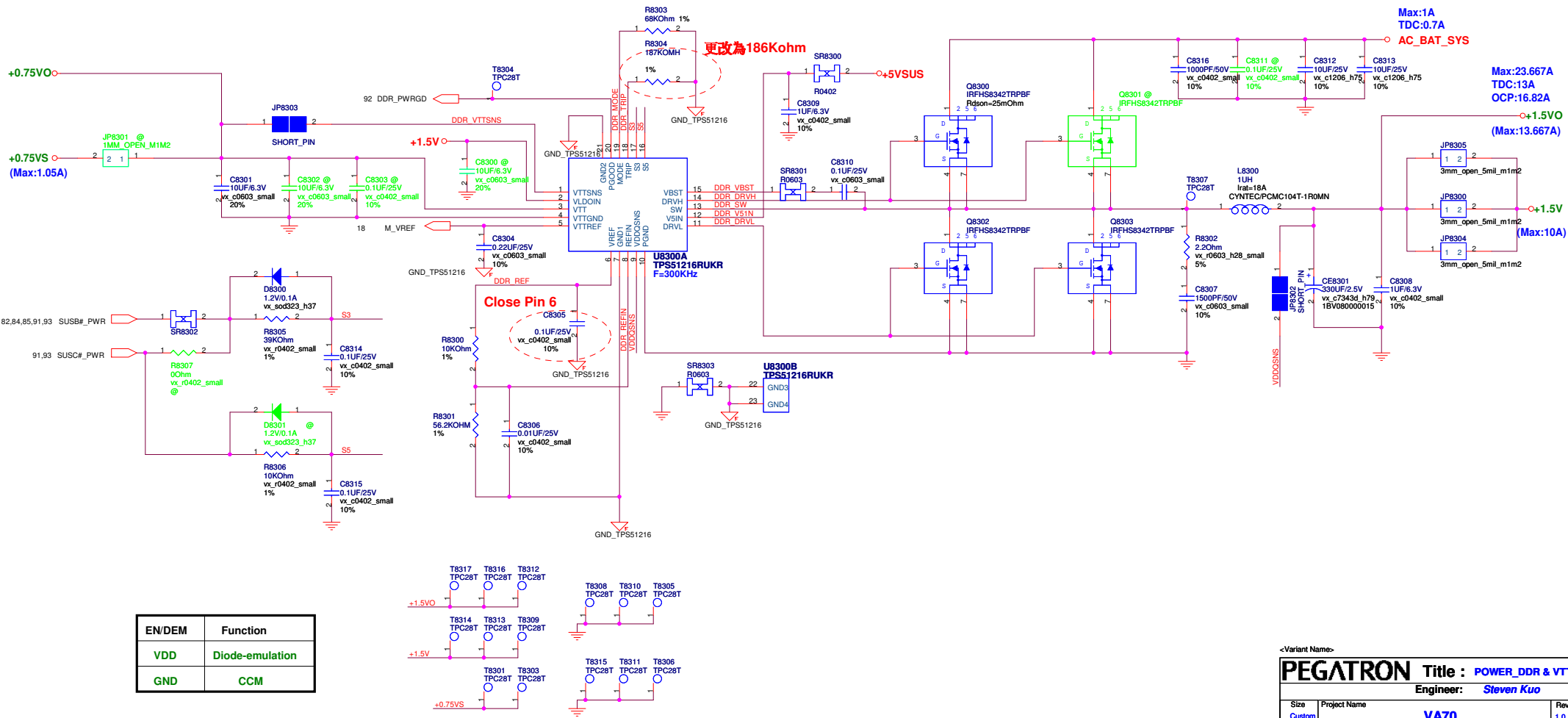


<Variant Name>					
PEGATRON		Title : POWER_SYSTEM			
		Engineer: Steven Kuo			
Size Custom	Project Name VA70				Rev 1.0
Date: Friday, February 03, 2012		Sheet 81 of 99			

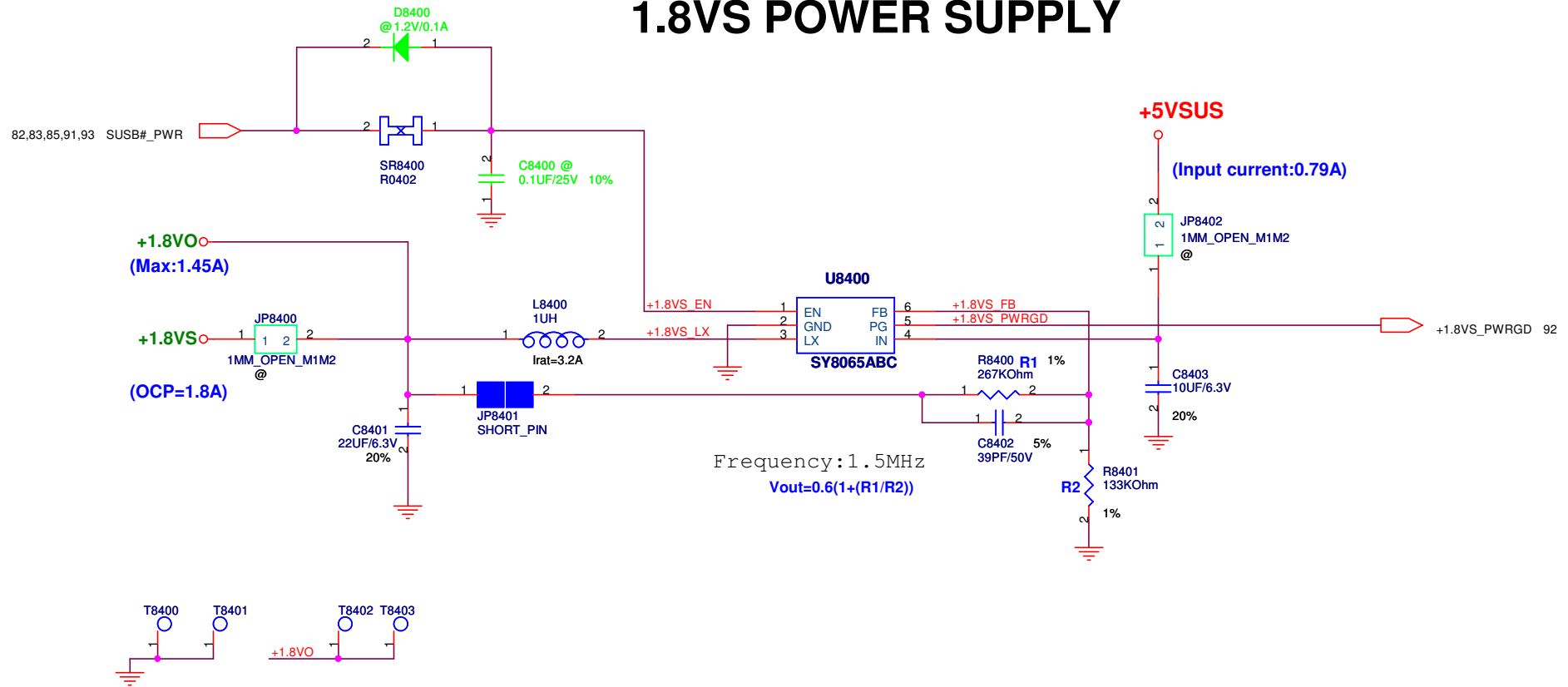
Used for testing purpose in production line.
Pull down to GND with a resistor of 470 kΩ or less



DDR & VTT POWER SUPPLY



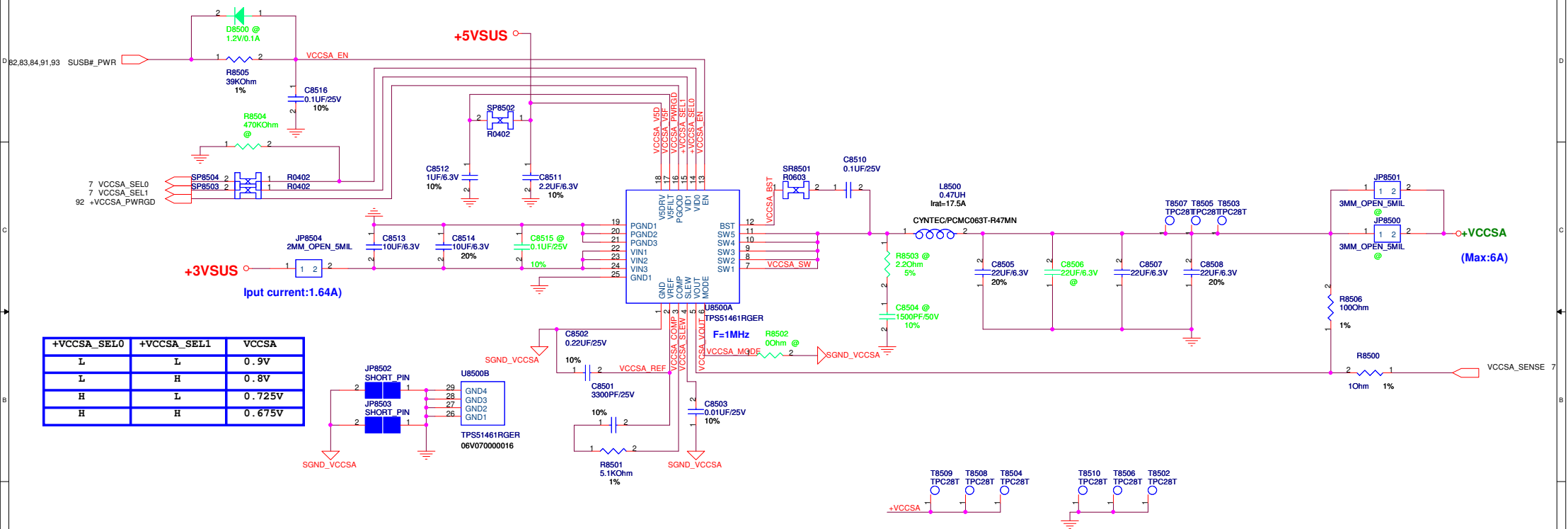
1.8VS POWER SUPPLY



<Variant Name>

PEGATRON		Title : POWER_1.8VS	
		Engineer: Steven Kuo	
Size Custom	Project Name VA70		Rev 1.0
Date: Friday, February 03, 2012		Sheet	84 of 94

VCCSA POWER SUPPLY



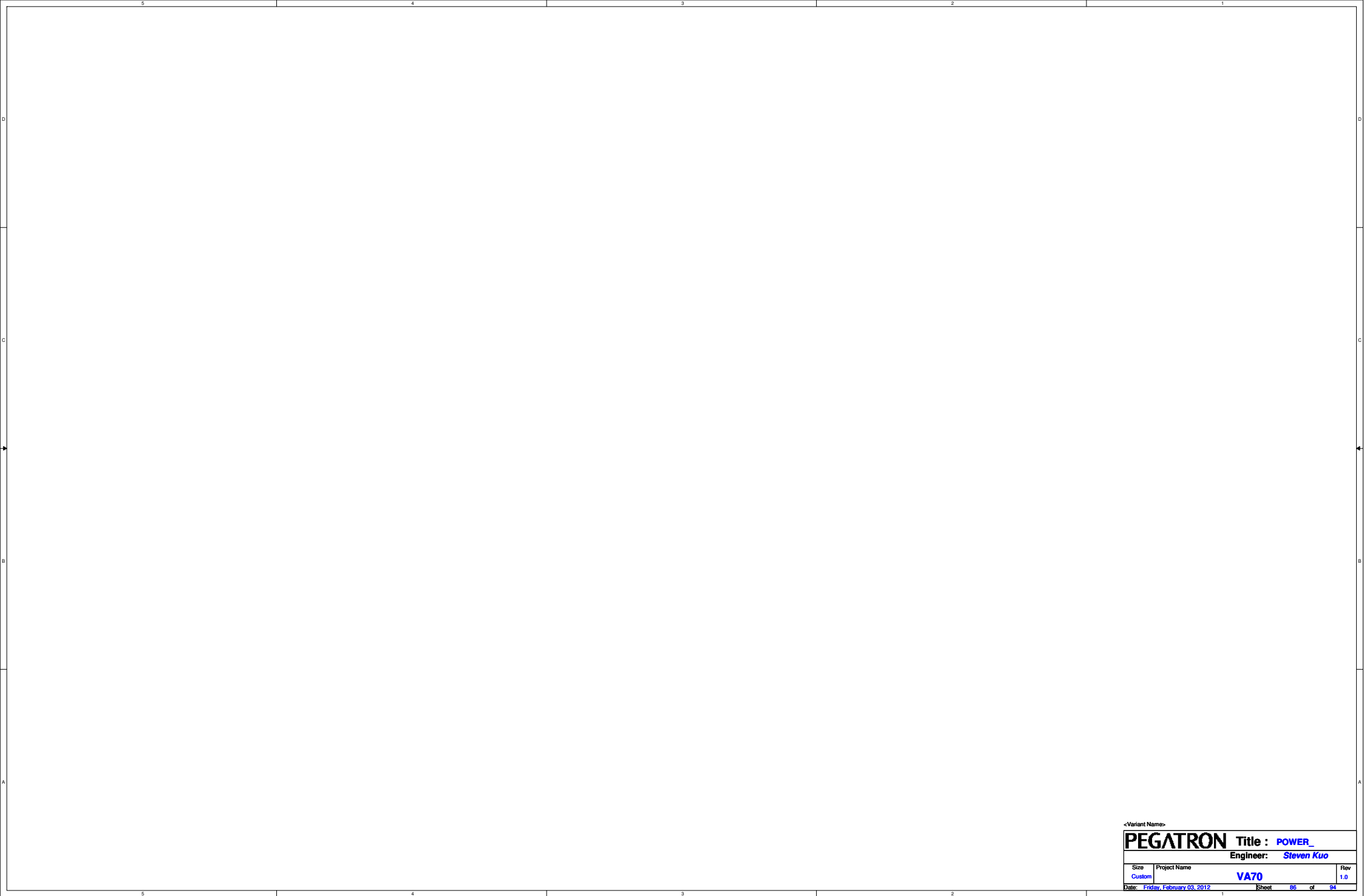
+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

<Variant Name>

PEGATRON Title : POWER_VCCSA

Engineer: *Steven Kuo*

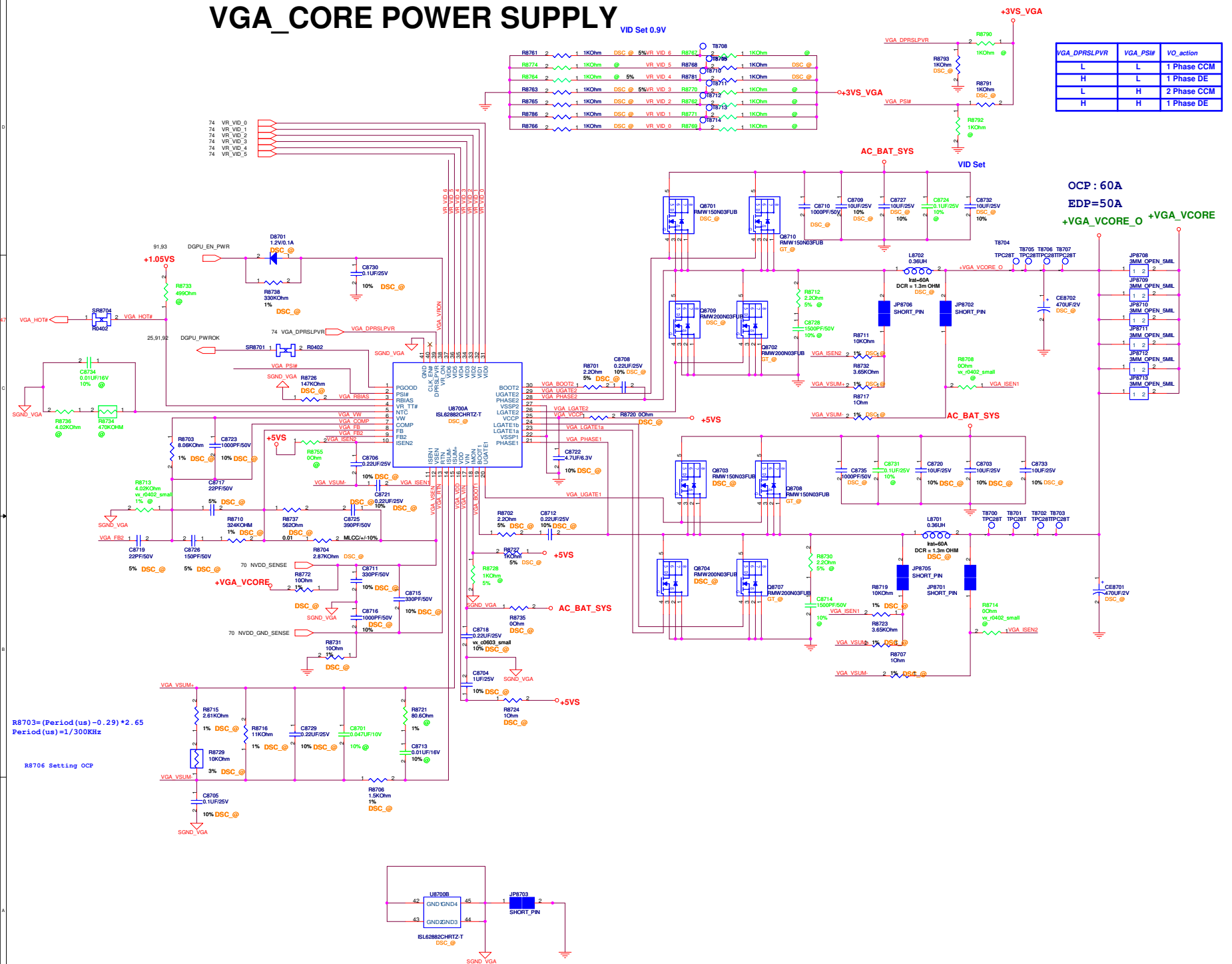
Size Custom	Project Name VA70	Rev 1.0
Date: Friday, February 03, 2012	Sheet 85 of 94	



<Variant Name>			
PEGATRON		Title : POWER	
		Engineer: Steven Kuo	
Size	Project Name		Rev
Custom	VA70		1.0
Date: Friday, February 03, 2012		Sheet	86 of 94

VGA_CORE POWER SUPPLY

VID Set 0.9V

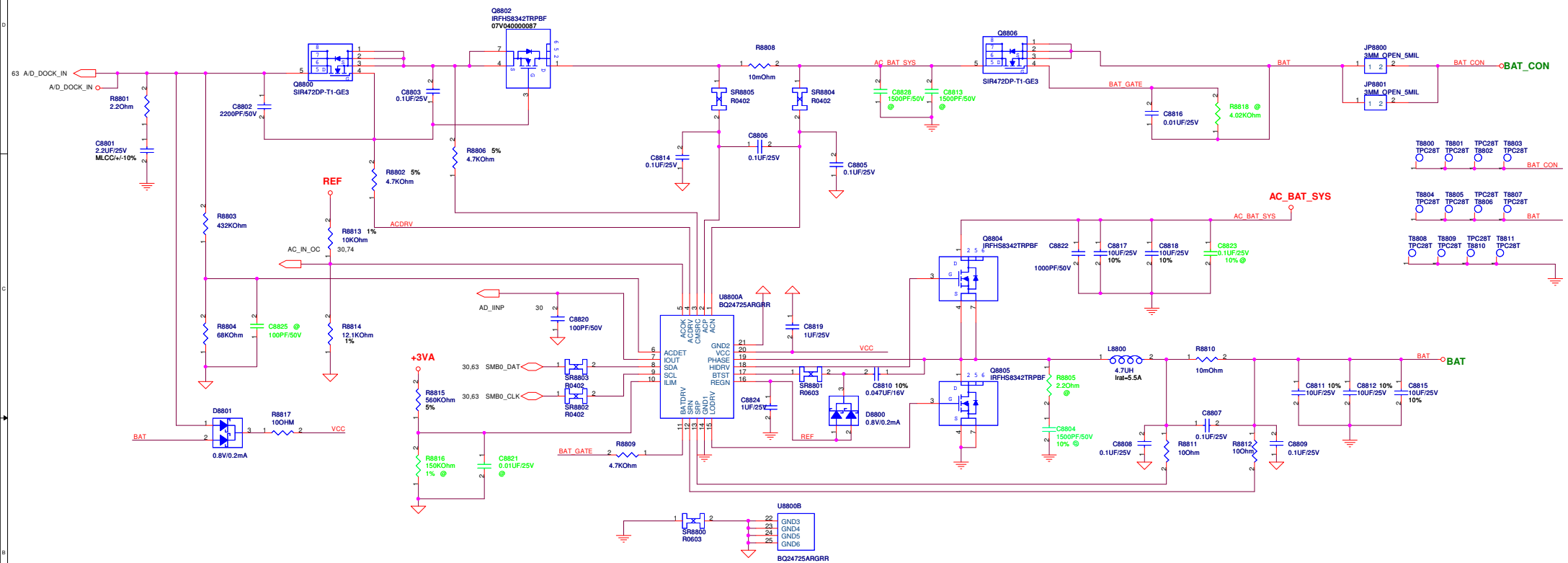


<Variant Name>

PEGATRON Title : **POWER_VGACORE**
Engineer: **Sтивен Kuo**

Size: **Custom** Project Name: **VA70** Rev: **1.2**
Date: **Friday, February 05, 2010** Sheet: **87** of **88**

BATTERY CHARGER



<Variant Name>

PEGATRON Title : POWER_CHARGER

Engineer: **Steven Kuo**

Size Custom	Project Name VA70	Rev 1.0
Date: Friday, February 03, 2012		Sheet 88 of 15

Date: Friday, February 03, 2012 Sheet 88 of 15

D

C

B

A

<Variant Name>

PEGATRON Title :POWER_N/A

Engineer:

Size	Project Name	Rev
A		1.1

Date: Friday, February 03, 2012 Sheet 89 of 99

5

4

3

2

1

5

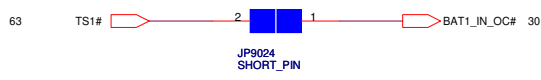
4

3

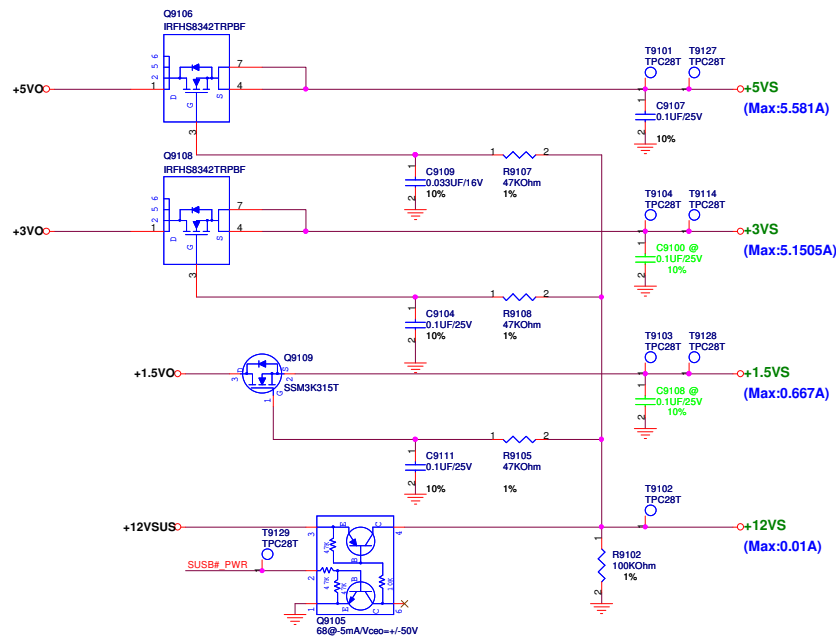
2

1

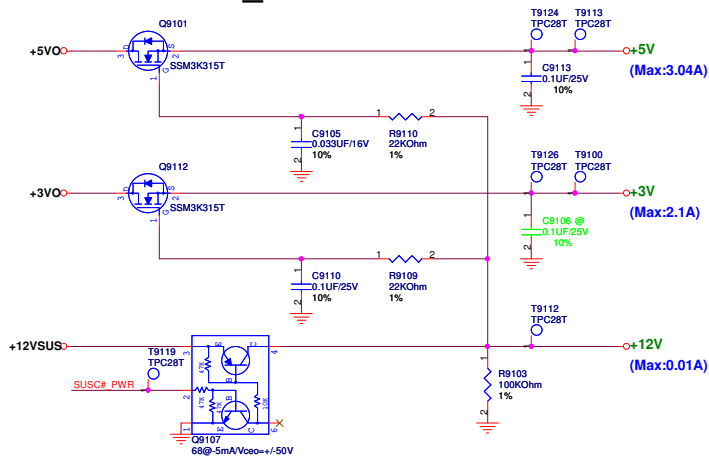
BATTERY IN DETECT



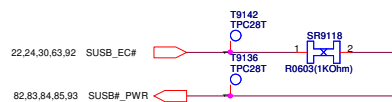
SUSB#_PWR POWER



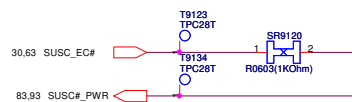
SUSC#_PWR POWER



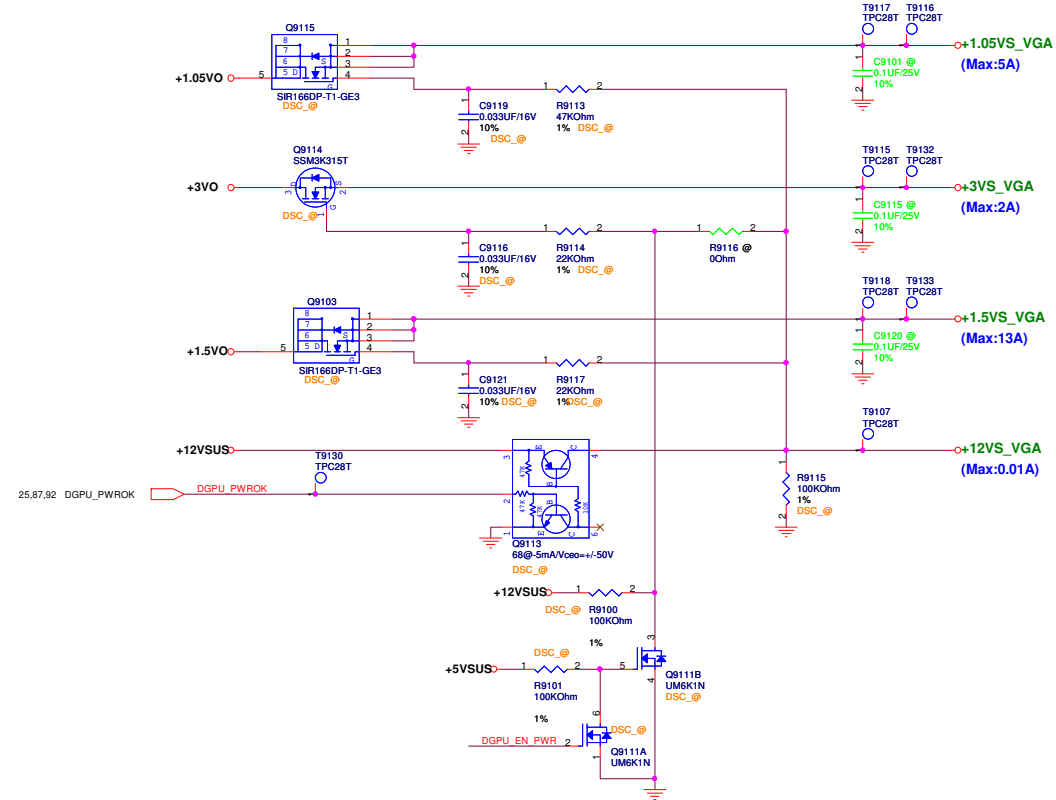
SUSB#_PWR POWER Control



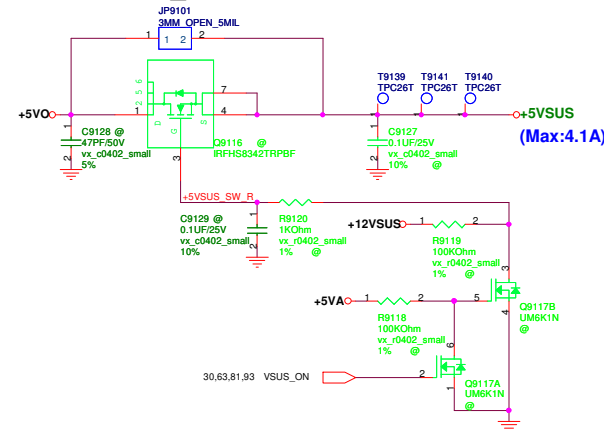
SUSC#_PWR POWER Control



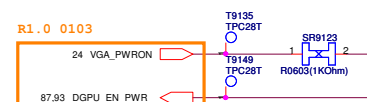
DSC#_PWR POWER(DGPU)



USBCHG#_PWR POWER

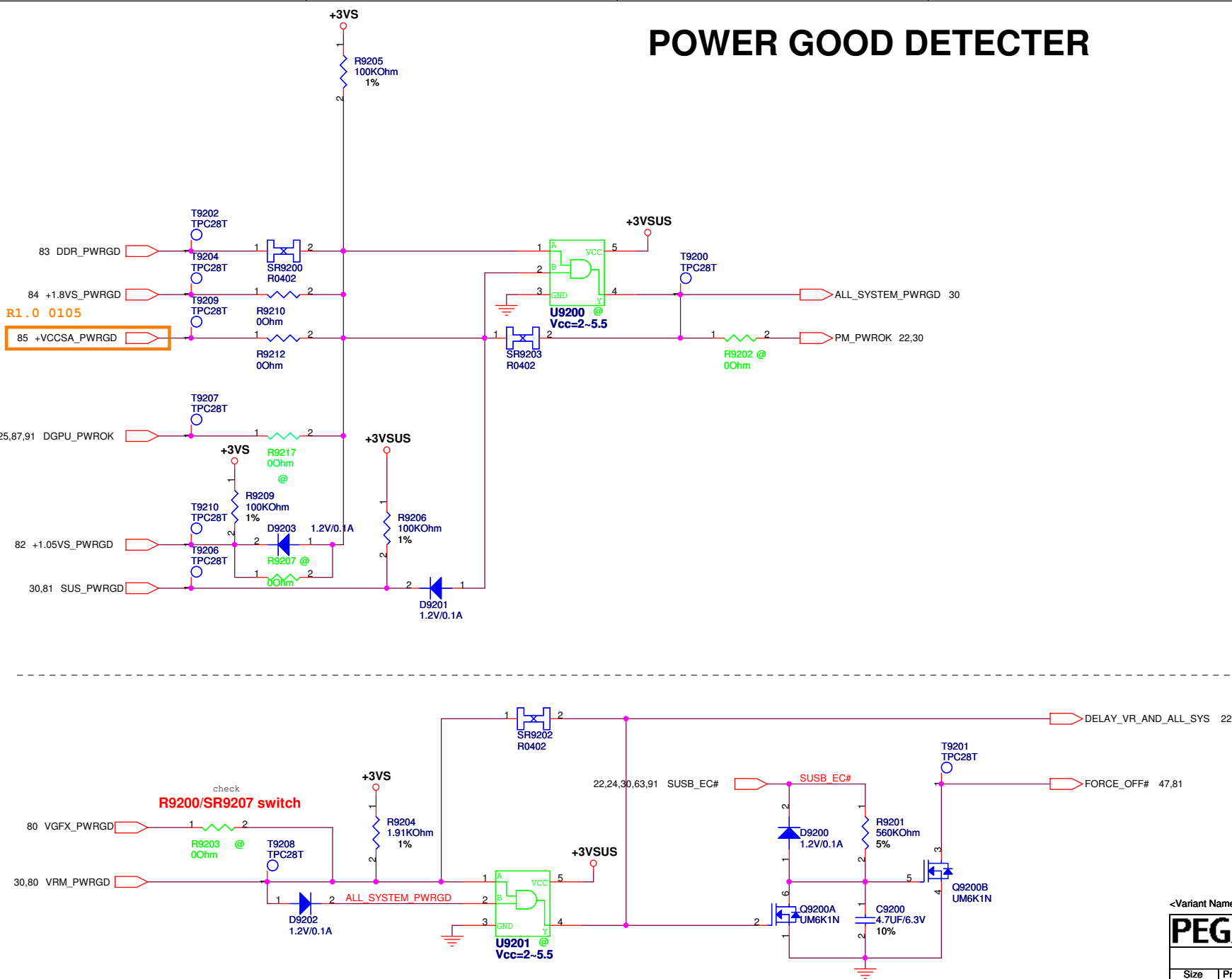


DSC_VGA_PWR POWER Control



<Variant Name>		Title : POWER_LOAD SWITCH	
PEGATRON		Engineer: Steven Kuo	
Size	Project Name	Rev	1.0
Custom	VA70		
Date: Friday, February 03, 2012	Sheet	91	of 94

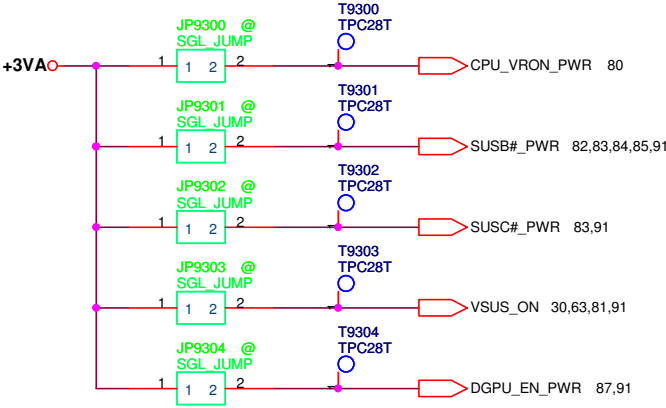
POWER GOOD DETECTOR



<Variant Name>		
PEGATRON Title : POWER_PROTECT		
Engineer: Steven Kuo		
Size Custom	Project Name VA70	Rev 1.0
Date: Friday, February 03, 2012	Sheet 92	of 94

AC_BAT_SYS		AC_BAT_SYS	37,55,80,81,82,83,87,88
BAT_CON		BAT_CON	63,88
+5VA		+5VA	30,42,61,66,81,91
+3VA		+3VA	20,27,30,48,63,65,81,88
+5VO		+5VO	61,81,91
+3VO		+3VO	55,81,91
+1.8VO		+1.8VO	84
+1.5VO		+1.5VO	83,91
+1.05VO		+1.05VO	82,91
+12VSUS		+12VSUS	22,28,60,81,91
+5VSUS		+5VSUS	22,27,30,60,61,63,65,66,82,83,84,85,91
+3VSUS		+3VSUS	4,22,24,27,28,30,33,65,81,85,92
+12V		+12V	91
+5V		+5V	51,63,91
+3V		+3V	4,24,37,51,63,65,91
+1.5V		+1.5V	5,7,16,51,63,83
+12VS		+12VS	28,39,41,91
+5VS		+5VS	27,30,38,39,41,42,48,49,60,63,66,80,87,91
+3VS		+3VS	4,16,17,20,21,22,23,24,25,26,27,28,30,37,38,39,40,41,47,48,49,53,55,60,63,66,69,91,92
+1.8VS		+1.8VS	7,25,26,63,84
+1.5VS		+1.5VS	26,53,55,63,91
+1.05VS		+1.05VS	26,27,63,80,82,87
+0.75VS		+0.75VS	16,17,63,83
+VCCSA		+VCCSA	7,85
+VCCP		+VCCP	3,4,6,7,25,26,27,37,47,63,82
+12VS_VGA		+12VS_VGA	91
+3VS_VGA		+3VS_VGA	63,70,72,74,75,87,91
+1.5VS_VGA		+1.5VS_VGA	63,71,75,76,77,91
+1.05VS_VGA		+1.05VS_VGA	63,70,71,72,91
+VGA_VCORE		+VGA_VCORE	63,75,87
+VGFX_CORE		+VGFX_CORE	7,63,80
+VCORE		+VCORE	6,63,80

FOR POWER TEST



<Variant Name>

PEGATRON		Title :	POWER_SIGNAL
		Engineer:	Steven Kuo
Size	Project Name		Rev
Custom	A35		1.0
Date: Friday, February 03, 2012		Sheet	93 of 94